

General Disclaimer

One or more of the Following Statements may affect this Document

- This document has been reproduced from the best copy furnished by the organizational source. It is being released in the interest of making available as much information as possible.
- This document may contain data, which exceeds the sheet parameters. It was furnished in this condition by the organizational source and is the best copy available.
- This document may contain tone-on-tone or color graphs, charts and/or pictures, which have been reproduced in black and white.
- This document is paginated as submitted by the original source.
- Portions of this document are not fully legible due to the historical nature of some of the material. However, it is the best reproduction available from the original submission.

INTERIM REPORT
Contract No. NAS8-32607
Supplemental Agreement No. 2

DESIGN, PROCESSING AND TESTING OF LSI ARRAYS

HYBRID MICROELECTRONICS TASK

28 SEPTEMBER 1978 - 27 MARCH 1979

15 APRIL 1979

Prepared for
George C. Marshall Space Flight Center
Marshall Space Flight Center
Alabama 35812

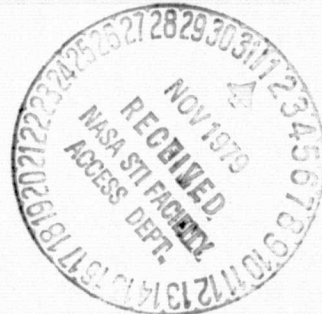
(NASA-CR-161312) DESIGN, PROCESSING AND
TESTING OF LSI ARRAYS: HYBRID
MICROELECTRONICS TASK Interim Report,
28 Sep. 1978 - 27 Mar. 1979 (Hughes Aircraft
Co.) 67 p HC A04/MF A01

N79-33396

Unclas
35982

HUGHES

SOLID STATE PRODUCTS DIVISION
NEWPORT BEACH, CALIFORNIA 92663



DESIGN, PROCESSING AND TESTING OF LSI ARRAYS
HYBRID MICROELECTRONICS TASK

INTERIM REPORT

28 September 1978 to 27 March 1979

Contract No. NAS 8-32607
Supplementary Agreement No. 2

Prepared for

GEORGE C. MARSHALL SPACE FLIGHT CENTER
MARSHALL SPACE FLIGHT CENTER, ALABAMA 35812

15 April 1979

R. P. Himmel
S. M. Stuhlberg
R. G. Ravetti
P. J. Zulueta

INDUSTRIAL ELECTRONICS GROUP

Solid State Products Division

Hughes Aircraft Company • Newport Beach, California 92663

CONTENTS

1.0	INTRODUCTION AND SUMMARY	1-1
2.0	TECHNICAL DISCUSSION	2-1
2.1	Task A - Cost Factors	2-1
2.1.1	Mathematical Models Refinement	2-3
2.1.2	Computer Programming and Models Verification	2-15
2.2	Task B - Tape Chip Carrier (TCC) Development ..	2-19
2.2.1	Tape Process Refinement	2-19
2.2.2	Wafer Bump Process Refinements	2-28
2.2.3	ILB Process Refinement	2-29
2.2.4	OLB Process Refinement	2-30
2.2.5	Test/Burn-in Process Refinement	2-36
2.2.6	Hybrid Microcircuit Applications	2-36
2.2.7	STAR Wafer Application	2-41
APPENDIX A	Cost Equation Summary	A-1
APPENDIX B	Program to Generate a Cost Surface and a Single-Valued Complexity Factor	B-1
APPENDIX C	Program to Generate a Single-Valued Cost Factor and Complexity Factor	C-1
APPENDIX D	Program to Generate a Single-Valued Cost Function and Complexity Factor by Means of a Portable Programmable Calculator ..	D-1

LIST OF ILLUSTRATIONS

Figure		Page
1-1	Overall Program Schedule	1-2
2-1	Cost Factors Program Schedule	2-2
2-2	Thin Film Substrate Fabrication	2-5
2-3	Thick Film Substrate Fabrication	2-6
2-4	Hybrid Microcircuit Assembly and Test	2-11
2-5	Hybrid Cost as a Function of Production Volume for Different Types of Facilities	2-13
2-6	Cost Surface of a Hybrid Microcircuit - Front View .	2-17
2-7	Printed Wiring Board Processing Sequence	2-18
2-8	Support Ring Concept	2-21
2-9	Polyimide Support Ring Formed by Special Tape Punching Tools	2-22
2-10	82-Pad ECL Device Mounted in Hermetic Chip Carrier via TCC Processing	2-23
2-11	Tape Processing Flow Chart	2-24
2-12	Hughes-Fabricated Photo Resist Exposure Unit	2-26
2-13	Gyrex Type 9 Microcoater	2-27
2-14	Plating Rack Designed Originally by Honeywell	2-27
2-15	Vertical and Horizontal Wafer Plating Concepts	2-29
2-16	IMI Mode 207 Inner-Lead Bonder	2-31
2-17	Combination Excise/Forming Tool Operation Diagram	2-32
2-18	Combination Excise/Forming Tool-Assembly Drawing	2-33
2-19	Hughes-IPD Manual Outer-Lead Bonder	2-34
2-20	Close-up Operation of Hughes-IPC Manual Outer- Lead Bonder	2-35

LIST OF TABLES

Figure		Page
1-1	Tape Chip Carrier Work Approach – Task B	1-6
2-1	Substrate Processing – Values of Constants and Parameters	2-7
2-2	Assembly and Testing – Values of Constants and Parameters	2-8
2-3	Line Width Factors	2-9
2-4	Non-Recurring Developmental Costs	2-12
2-5	Non-Recurring Manufacturing Costs	2-12
2-6	Production Facility Factor (γ)	2-14
2-7	Reference Hybrid Parameters	2-15
2-8	Example of TCC Tape Punch-Out Connection Sequence	2-39

1.0 INTRODUCTION AND SUMMARY

This report summarizes the first six months of effort on Contract NAS 8-32607, Supplementary Agreement No. 2; a continuation of the 1977-1978 cost-factors/packaging program. Specifically, this program involves determination of those factors affecting the cost of electronic subsystems utilizing LSI microcircuits, and development of the most efficient methods for low-cost packaging of LSI devices as a function of density and reliability. Overall program progress is summarized in Figure 1-1.

This one-year supplementary program has been divided into two Tasks as follows:

TASK A - Cost Factors Study

Mathematical cost factors were generated under the original contract for both hybrid microcircuit and printed wiring board (PWB) packaging methods, and a mathematical cost model was created for analysis of microcircuit fabrication costs. Under the Supplementary Agreement effort, the cost model is to be refined and broadened to cover discrete (PWB) packaging techniques, and to include component parts such as ceramic chip carriers, multichip LSI "subassembly" arrays, and plastic LSI packages (all of which may incorporate tape chip carrier interconnection technology). The costing factors previously developed are to be refined and reduced to formulae for computerization.

TASK B - Tape Chip Carrier Development Study

Tape chip carrier technology has been shown under the original contract to represent a viable approach to low cost LSI packaging, with additional potential for lowering the cost of hybrid microcircuit fabrication. Certain technical problem areas, inherent to LSI applications, have been identified; work is to continue during the Supplementary Agreement time period in an effort to resolve these problems by continued development in the areas of wafer bumping, inner/outer leading bonding, testing on tape, and tape processing.

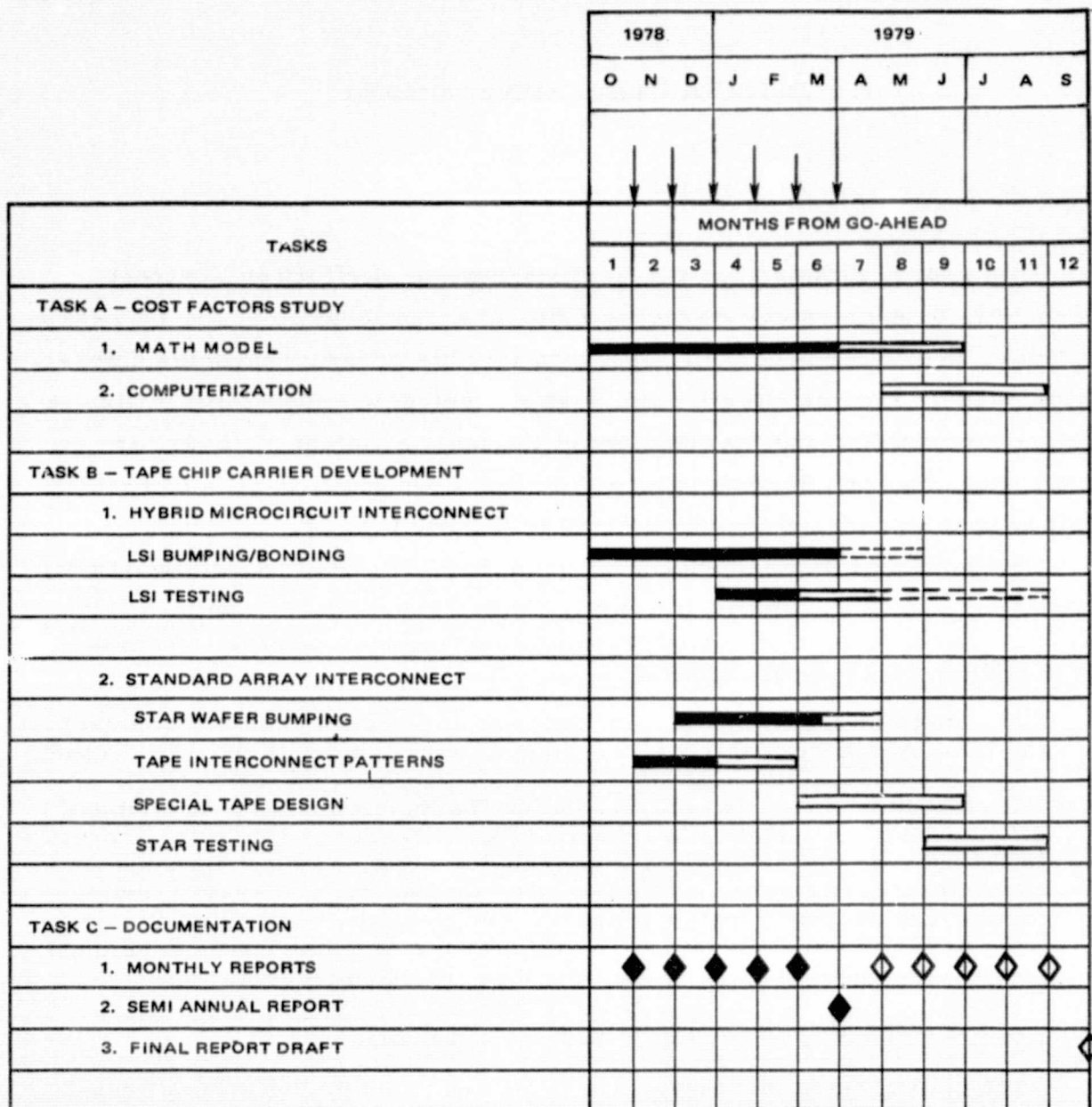


Figure 1-1. Overall program schedule.

Task B (Continued)

Tape chip carrier technology shall be developed further by studies and laboratory effort toward demonstrating the feasibility of inter-connecting arrays of two, four, or more LSI chips on the tape carrier. Such arrays would form standard modules or "blocks", from which larger assemblies could be constructed.

TASK A Synopsis

Mathematical cost models previously developed for hybrid micro-electronic subsystems have been refined and expanded under Task A during this reporting period to include rework terms related to substrate fabrication, non-recurring developmental and manufacturing operations, and prototype production. In addition, sample computer programs have been written to demonstrate hybrid microelectronics applications of these cost models, and processes for printed wiring board (PWB) fabrication have been modeled.

The mathematical equations which have been reported under the original contract (Final Report No. P78-549, dated 15 September 1978), were derived by collecting cost factors relevant to the manufacturing processes of hybrids, and by expressing them in terms of process and component parameters.

The purpose of this work is to develop a tool to evaluate the entire hybrid microelectronics fabrication cost when technological changes are made in any portion of the processes involved. In this way, those changes which are associated with cost reductions will become more readily identifiable; currently, they are hidden in the literature, or in the practical knowledge of a few qualified people.

The ability to predict cost consequences when a change in technology is made is a major factor in bringing about reduced production costs. Coincidentally, in seeking cost savings, new technological approaches are derived. The models therefore will have served their purpose if, besides identifying those areas which will impact cost savings directly, they also help to identify those additional technological improvements necessary to cause further savings.

The models previously developed were valid only when applied to volume runs on the order of 120,000 units yearly. Improvements of these mathematical cost models during this time period included the following areas:

1. Substrate fabrication
 - a. Rework cycles and inspection steps have been added.
 - b. The yield of the fabrication process has been expressed in terms of rework.
2. Total hybrid microelectronics subsystem fabrication
 - a. Non-recurring developmental and manufacturing costs have been included in the equations.
 - b. Production volume has been introduced as a variable parameter in the equations.
 - c. The values of constants, and those parameters defining the reference hybrid, have been reestablished to include prototype production.

A simplified version of the equation expressing the total cost of a hybrid microcircuit has been computerized as an example, and used to generate a three-dimensional surface. A graphical display such as this is better understood and more readily related to personal experience than is any other display form.

In addition to these cost factors improvements, PWB fabrication flow charts have been modeled, utilizing only the most economically and technologically significant steps of the processes involved.

TASK B Synopsis

Task B has two basic parts. In the first part, developmental work has continued on LSI packaging utilizing tape chip carrier technology, particularly in the areas of tape processing, wafer bumping, and inner/outer lead bonding. In the second part, studies and laboratory efforts have been initiated to show the feasibility of interconnecting arrays of LSI chips utilizing tape chip carrier and semi-automatic wire bonding technology.

Table 1-1 is a work approach matrix which outlines the tape chip carrier tasks completed under the original contract, and which indicates the direction of effort which has been undertaken during the Supplementary Agreement time period on a Task/Goal basis. Specific semiconductor device types are listed and identified by code letter.

Subtask Numbers 8 (Lead Finger Support) and 12 (Silicon Nitride Coating/Retest) were included for target or "best efforts" investigations as time and funding considerations permit. The "Lead Finger Support" task covers several techniques/materials which Hughes has been investigating on internal funding during the program time period. This concept involves potential tape carrier yield improvements brought about by inclusion of a soluble organic etched-lead support within the window area.

The Silicon Nitride Coating/Retest effort refers to a current U.S. Air Force (AFML) Manufacturing Technology Program with Hughes-Culver City (Contract F33615-78-C-5049), in connection with which Hughes-Newport Beach currently is conducting reliability investigations. A production reactor offering relatively-low-temperature (150°C) Si_3N_4 coating of hybrid microcircuits, tape-carrier-mounted devices, and packaged semiconductors is scheduled for installation in the Newport Beach facility during June, 1979.

Under Subtask 13, studies and developmental effort are being applied to the interconnection of standard array LSI devices, in groups of two, four, or more, in an effort to bring about a cost effective and versatile packaging method for minicomputers and high density memory arrays.

One example of a standard array device, and the type planned as a test vehicle for this developmental effort, is the NASA-developed STAR (Standard Transistor Array Radix). The STAR design system is a double-metal semi-custom approach to generating quick-turnaround MOS digital LSI circuits. It consists of an array of devices defined in different technologies with a common grid system. The arrays are processed to the point of metal definition and held in storage. STAR circuit interconnection designs are created by three custom masks that define the first level of metal, the via mask, and the second level of metal. The STAR has been defined by NASA in the CMOS-BULK metal gate, CMOS-SOS silicon gate, CMOS-BULK silicon gate, CCL-SOS, and CCL-BULK technologies. A family of 22 logic

TABLE 1-1. TAPE CHIP CARRIER WORK APPROACH - TASK B

TAPE CHIP CARRIER WORK APPROACH - TASK B

Task Description	Planned Device Complement	Program Goals	Planning/Execution			
			25	50	75	100
1. Wafer Bumping	B, C, D, E, G	More Definitive Process Refinement Required				
2. Wafer Characterization (Before/After Bumping)	D, E	To be Conducted Jointly with Suppliers				
3. Tape Preparation	D, E, and G (A, B, C as required)	Expansion to 6-in. and/or 12-in. Lengths				
4. ILB	D, E, and G (complete C)	Use of Projected New IMI Production Bonder				
5. Testing on Tape	D, E, and G (complete C)	Functional Testing				
6. Burn in on Tape	A (possibly D and E)	Demonstration				
7. Excise/Forming	D, E, and G (complete C; Excise only for HCCs)	C: Use Newly-Received Tool; Procure New Tool				
8. Lead Finger Support	B, C, D, E, and G (best efforts)	Investigate for ILB Compatibility, Solubility				
9. OLB to S/F Networks	A and G	Multilayer Circuitry				
10. OLB to HCCs	Complete B and C; possibly D and E	Process Demonstration, Refinement				
11. Reliability Testing of Networks/HCCs	E (possibly B and G)	Pressure Cooker Test, Thermal Cycling, HTRB; Both HCCs and Networks				
12. Silicon Nitride	Best Efforts: A, B, C, D, E, and G	Potential Replacement for Hermetic Packages				
13. Multiple-Chip TCC or Wire-Bond	Best Efforts: E	Initial Conceptual Investigation and Proof-of-Performance				

Planned Devices:

A: 14-Pad Type 5400/54LS00 Dual Quad NAND Gates (Fchld.)

B: 18-Pad Type 1824D Microprocessor RAM (HAC)

C: 82-Pad ECL/MUX, ECL/REG, and/or ECL/MAA (Sig.)

D: 40-Pad Type 6402 CMOS UART (Harris)

E: 38-Pad 384-Element STAR (MSFC)

F: 64-Pad 1584-Element STAR (MSFC)

G: 35-Pad Type 342 CMOS Digital Correlator (HAC)

cells have been designed and digitized by NASA for use with STAR arrays, which are being created in different sizes, from 384 transistors up to 5264 transistors.

STAR technology offers many advantages of custom integration such as reliability, secrecy, power, and size reduction, but allows faster turn-around time and lower cost than that possible with custom integration techniques. In Subtask 13, the objectives of low cost and fast turn-around will be extended to the next level: packaging of STAR devices.

Section 2.0 includes a description of Task A and B progress during the time period covered by this report.

2.0 TECHNICAL DISCUSSION

Mathematical model refinement under Task A largely has been completed, as indicated in Section I and summarized in the Cost Factors Program Schedule of Figure 2-1. Considerable Tape Chip Carrier (TCC) process refinement progress has been made under Task B; bump processing of the 1.5-inch-diameter x 0.008-inch mechanical sample STAR wafers received from MSFC has been delayed however, because of breakage problems during handling.

2.1 TASK A - COST FACTORS

Substrate fabrication flow charts for thin and thick film technology have been modified to include inspection/quality-control steps and rework cycles. The addition of rework cycles in the models permits process yield expression on an explicit basis, thus eliminating the previous need for defining an additional yield parameter independent of process parameters.

Equations representing substrate (network) fabrication consequently have been modified by the addition of two new parameters: (a) Inspection cost, and (b) Number of rework cycles; in addition to introduction of new coefficients.

The previously-developed mathematical models were applicable to large production quantities (about 120,000 per year). It consequently was necessary to modify these models so that the total cost of a hybrid could be predicted when small production quantities are considered (one to 1500 per year, in lot sizes of one to 100).

The generalization to include small production quantities was made by means of the following two steps: a) Additional cost factors were gathered

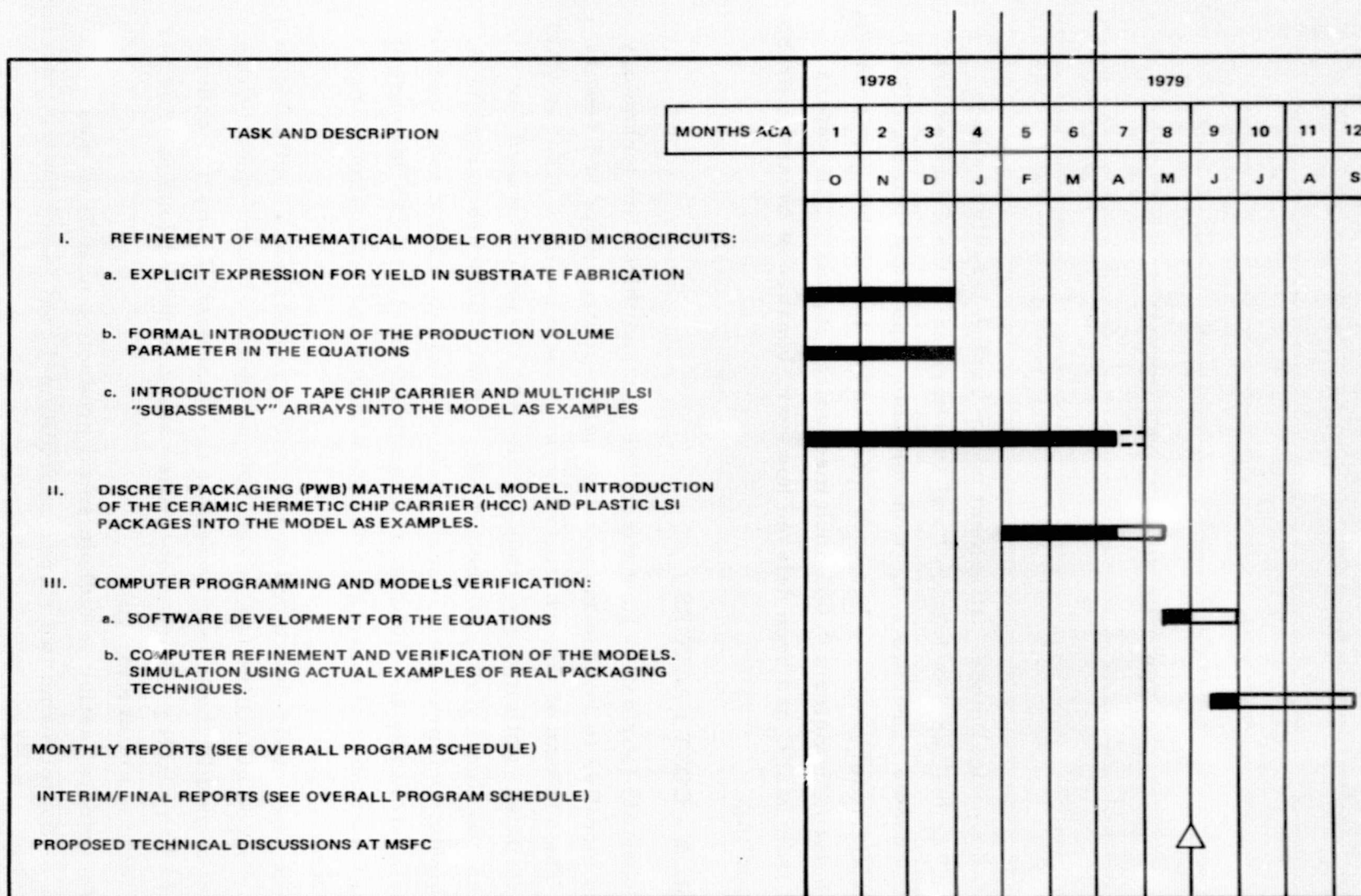


Figure 2-1. Cost factors program schedule

concerning the production of hybrids in prototype facilities and, b) These costs were introduced as additional terms (and/or multiplying factors) in previously-developed equations.

As a consequence of this generalization, it was found that differentiation of engineering costs between a hybrid built in a prototype facility, and the same hybrid built in a large production facility, was an important consideration. Differences between these hybrids have been expressed quantitatively in graphical form by using a family of curves; and in symbolic form by means of distinct equations. The equations were obtained with the data available by finding the best curve fit using a statistical analysis approach.

In addition to the above-described factors, distinction has been made between recurring and non-recurring costs. These costs now are expressed in the equations as percentages of total manufacturing costs. In this way, the non-recurring engineering costs proportionally change with the total manufacturing cost, and they are affected directly by the degree of hybrid complexity.

Three major categories have been considered for the non-recurring developmental costs: a) Engineering costs, which include items such as applications engineering, design layout, package drawings, and test fixtures design; b) Engineering Proof of Design (POD) models, which include planning for the continuation of production, engineering support, and total fabrication/assembly; and c) Engineering Pre-Production Models, which take into account the costs necessary to build exactly the same hybrids that will be required in production.

Items such as test fixtures, layouts, masks, manufacturing drawings, screens, and instructive photos have been introduced into equations as part of the non-recurring manufacturing costs.

2.1.1 Mathematical Models Refinement

In refining the mathematical models developed during this program, substrate processing has been considered as a separate sub-category, which then becomes a factor of the total Hybrid Microelectronics Subsystem Cost.

2.1.1.1 Substrate Processing

The cost, in dollars, of thin or thick film substrate processing, C_{SP} , is modeled by the following equation:

$$C_{SP} = (1 + a' + b') [C_S + (C_p + C'_{QC}) W_R] + (1 + b') (C_U + C_{RT} + C_{QC}) W_R \quad (1)$$

where a' and b' are integers expressing the number of times that the substrate has been rejected by inspection before and after resistor trimming, and W_R is an arbitrary wage rate constant in dollars/hour. The other symbols in the quotation are identified with steps in the flow charts of Figures 2-2 and 2-3, (for thin and thick film substrate fabrication, respectively). The other costs are in standard hour (STDH) units.

Equation 1 can be rewritten as:

$$C_{SP} = (1 + a' + b') C_{OS} S_Z + (C_{OE} C_C \ell_W + K'_{QC} C_C S_Z) W_R + (1 + b') (C_U + K_T \delta_{SR} \delta_R t_R + K_{QC} C_C S_Z) W_R \quad (2)$$

Symbol meanings can be found in Tables 2-1 and 2-2. The two new terms C_p and C'_{QC} , which are introduced as a consequence of explicitly expressing the rework, are defined below:

- a. Circuit photoetching processing - Assume this cost, C_p , to be a function of the circuit complexity, C_c , and of circuit line width factor, ℓ_W . Define as

$$C_p = C_{OE} C_C \ell_W$$

The line width factor ℓ_W is reported in Table 2-3 for thin and thick film processes.

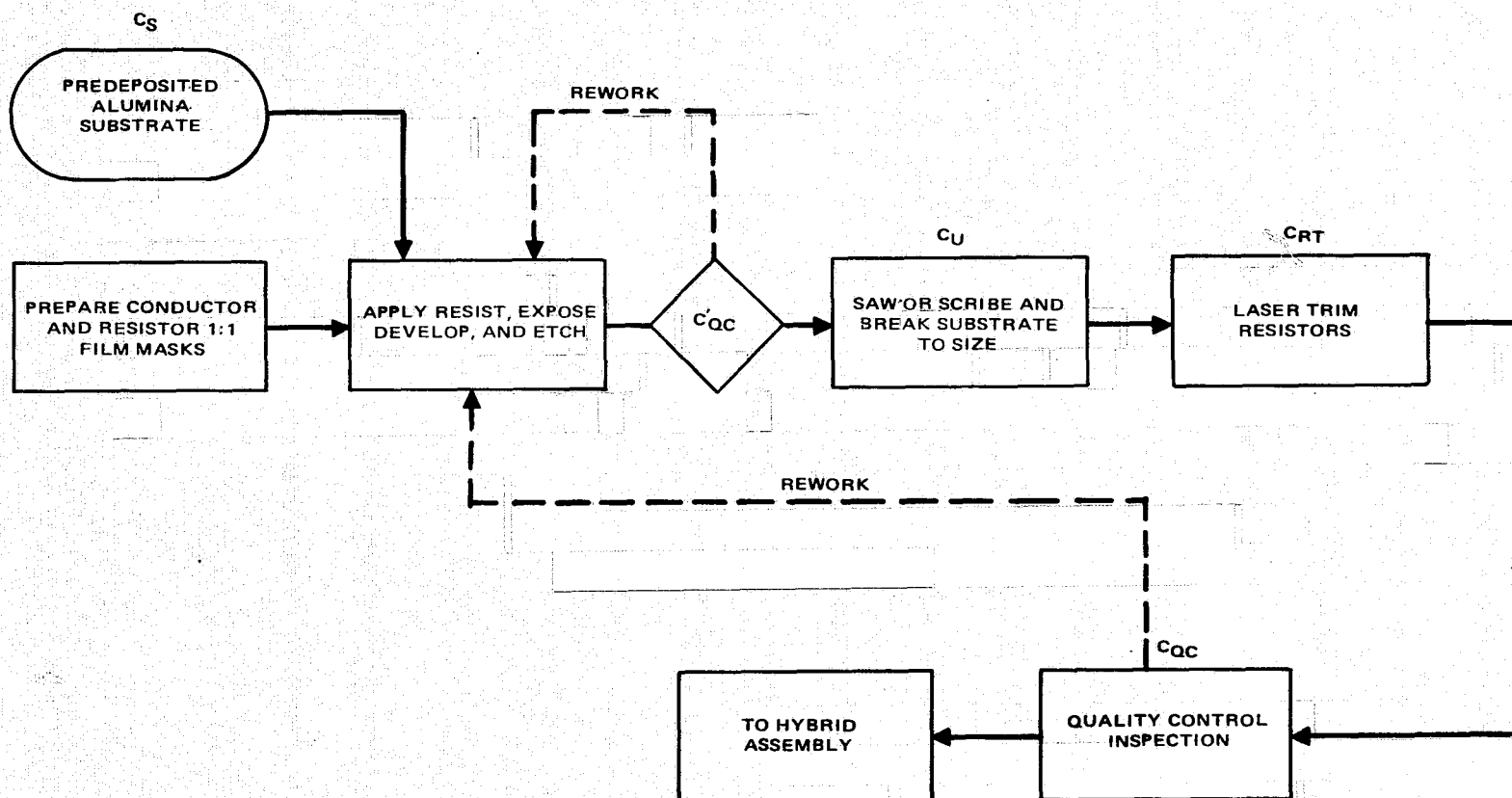


Figure 2-2. Thin film substrate fabrication

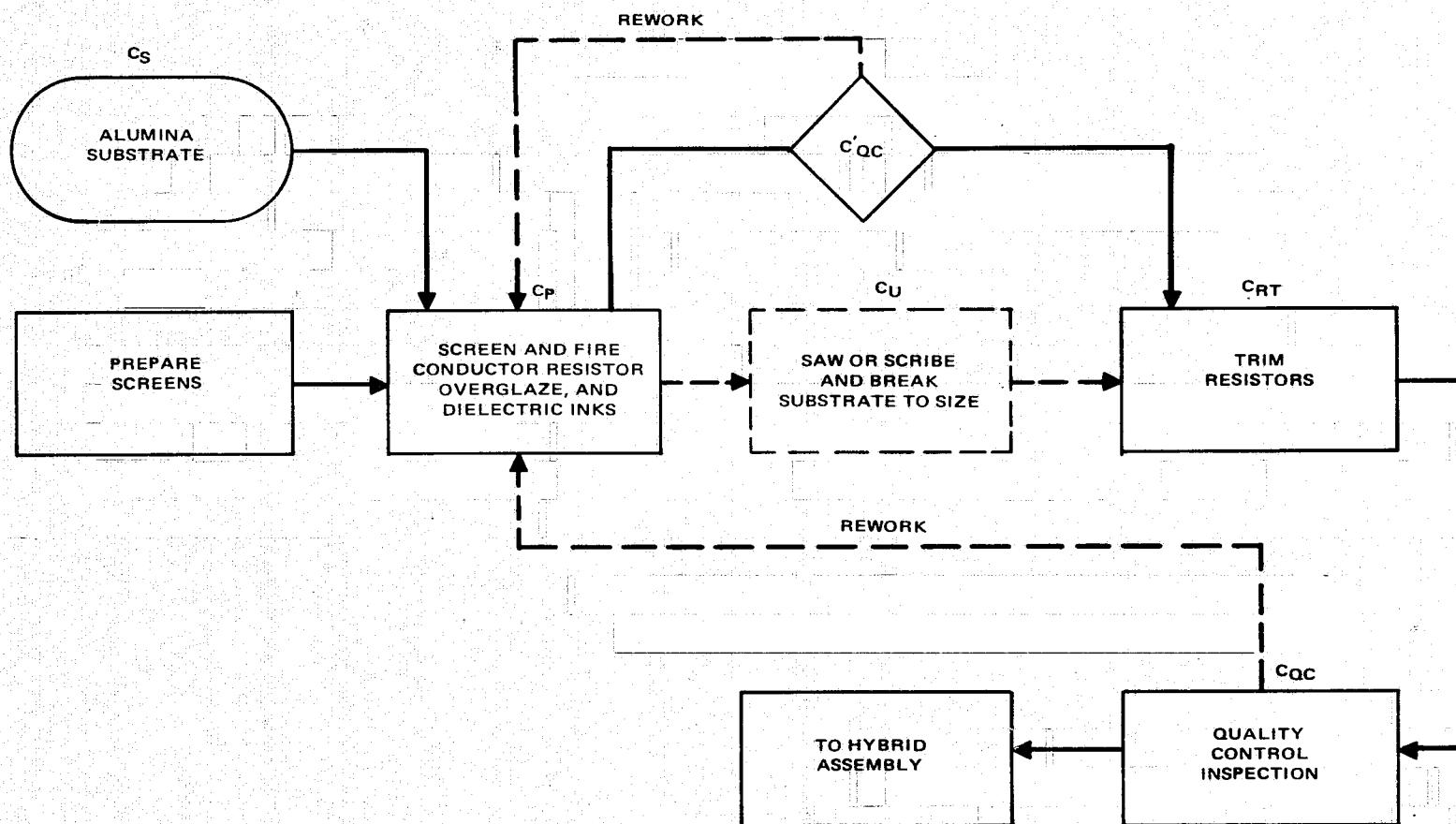


Figure 2-3. Thick film substrate fabrication

TABLE 2-1. SUBSTRATE PROCESSING - VALUES OF
CONSTANTS AND PARAMETERS

	Constants	Thin Film	Thick Film
C_{OS}	Dollars	30.00	0.64
C_{OE}	Standard Hours (STDH)	0.124	0.024
K_T	$STDH \times \ln^2$	0.205	0.038
K_{QC}	STDH	7.2×10^{-2}	4×10^{-2}
K_C	\ln^2	6×10^{-3}	1.36×10^{-2}
K'_C	Non-dimensional	7.5×10^{-3}	7.5×10^{-3}
K'_{QC}	Non-dimensional	7.2×10^{-2}	4×10^{-2}
	Parameters	Thin Film	Thick Film
ϕ_R	Number of Resistors/ \ln^2	23	8
ϕ_c	Number of Chips/ \ln^2	34	17
ϕ_{SR}	Area of one Resistor Hybrid Area	5.4×10^{-4}	2.28×10^{-3}
t_R	Inverse of Tolerance	5	5
S_Z	Hybrid Size Factor	1.0 for 1.5 x 2-Inch Substrate; 0.5 for 0.75 x 1.75-Inch Substrate; 0.3 for 1 x 1-Inch Substrate	
C_c	Hybrid Complexity Factor (Medium-Complexity)	0.5	
ϕ_{pmax}	Maximum Number of Pads found on 1C	16	
W_r	Wage Rate (Arbitrary Constant Assigned for Relative Comparison Only), \$/Hr	12.00	

- b. QC Inspection - Assume this cost, C'_{QC} , to be a function of circuit complexity C_C and hybrid size factor S_Z . Define as

$$C'_{QC} = K'_{QC} C_C S_Z$$

TABLE 2-2. ASSEMBLY AND TESTING - VALUES OF
CONSTANTS AND PARAMETERS

<u>Constants</u>			
C _{OP}	Dollars	23	
β ₀	Non-Dimensional	7×10^{-6}	
β ₁	Dollars	0.13	
β ₂	Dollars	0.80	
β ₃	Dollars	1.6	
C _{OPT}	Standard Hours (STDH)	0.033	
a	STDH	9.3×10^{-4}	
b	STDH	6.6×10^{-4}	
d	STDH	0.0033	
K _{QC1}	STDH	0.088	
g	STDH	0.088	
g'	STDH	2.76	
h	STDH	0.025	
K _{QC2}	STDH	0.51	
l	STDH	0.186	
C _{TT}	STDH	0.22	
g''	STDH	1.38	
h'	STDH	0.044	
K _{QC3}	STDH	0.02	
C _o	STDH	0.25	
u	STDH	0.0275	
u _B	Dollars	0.20	
<u>Parameters</u>			
		<u>Thick Film</u>	<u>Thin Film</u>
N _{TRJ}	Total Number of IC Transistor Junctions	480	240
N _{TRD}	Total Number of Transistors and Diodes	13	6
N _{CAP}	Total Number of Capacitors	20	10
N _C	Total Number of Chips	45	22
N _{CIC}	Total Number of ICs	12	6
N _{WB}	Total Number of Bonds	640	340
N _R	Total Number of Resistors	30	10
t _y	Package Type Factor (Figure 2-4)	2.0 for Butterfly Package 1.0 for HAC-PAC	
Q	Number of Packages Purchased in a Lot	10,000	
C' _L	Average Cost of a Package Lid	\$1.70	
n _l	Number of Lids	1.0	
C _{BS}	STDH for Substrate Bonding	0.12	

(Continued next page)

(Table 2-2, continued)

	Parameters	Thick Film	Thin Film
m	Die Attachment Factor	1.0 for Epoxy Attachment 2 for Moly Tab Attachment	
ϵ_p	Number of Pads/IC	14	
f	Fraction of Other Connections (Jumpers and to Package Leads)	0.40	
r	Reliability Level Factor	1 for Military or Space 0 for Low and High Cost	
N_{TRJ}	Average Number of Transistor Junctions/Chips	40	
η	Number of Reworks Before Sealing	1	
η'	Number of Reworks after Sealing	1	
g_1	Fraction of Chips Reworked Before Sealing	0.1	
g_2	Fraction of Bonds Reworked Before Sealing	0.05	
g'_1	Fraction of Chips Reworked After Sealing	0.02	
g'_2	Fraction of Bonds Reworked After Sealing	0.004	
C_{LR}	Rework Due to Lid Substitution, STDH	0.20	
C_{TT}	Acceptance Test, STDH	0.25	
V	Number of Hybrids Produced Per Year	1.2×10^5	
a'	Number of Reworks Before Resistor Trimming	1	
b'	Number of Reworks After Resistor Trimming	0	

TABLE 2-3. LINE WIDTH FACTORS

Line width factor l_w	Line Width, inches					
	Thin Film			Thick Film		
	0.01	0.005	0.002	0.025	0.015	0.007
	0.75	1.00	3.00	0.75	1.00	3.00

2.1.1.2 Total Hybrid Microelectronics Subsystem Cost

The total cost for a hybrid (C_H) is given in dollars by

$$C_H = C_M + (C_{SP}^o + C_{AT}^o) P(p_1, p_2, C_C) F(V), \quad (3)$$

where C_M is the cost of materials necessary to build one hybrid. C_{SP}^o is the manufacturing cost of the thin or thick film substrate, and C_{AT}^o is the manufacturing cost of the assembly and testing (derived from modelling the process as shown by the flow chart of Figure 2-4. $P(p_1, p_2, C_C)$ is a function which represents the non-recurring developmental (p_1) and manufacturing (p_2) costs, and $F(V)$ is a function which takes into account the quantity of hybrids produced in one year by a production facility.

The functional relationship $P(p_1, p_2, C_C)$ is expressed mathematically by

$$P = (p_1 + p_2) C_C. \quad (4)$$

The factors p_1 and p_2 are given by Tables 2-4 and 2-5 respectively. Eventually, where a detailed cost breakdown is necessary, p_1 and p_2 can be expressed as a summation of the cost factors breakdown which also is shown in Tables 2-4 and 2-5.

Functionally, $F(V)$ is expressed by an equation of the type $F(V) = \gamma V^{-\beta}$, where $\beta = -0.4$ is the slope of the curve cost versus volume in log-log representation.

Three curves representing different types of production facilities are reported in Figure 2-5. The need to separate the production of hybrids into three categories is dictated by manufacturing organizational criteria. In fact, to produce a hybrid in a facility which is not properly equipped is a waste of time and money.

The factor β is the same for all three curves, since the slope is the same for all of them, but the factor γ is different for each curve. This factor identifies which production facility (low, medium, or large volume) produces the hybrid microelectronic units. The different values for γ

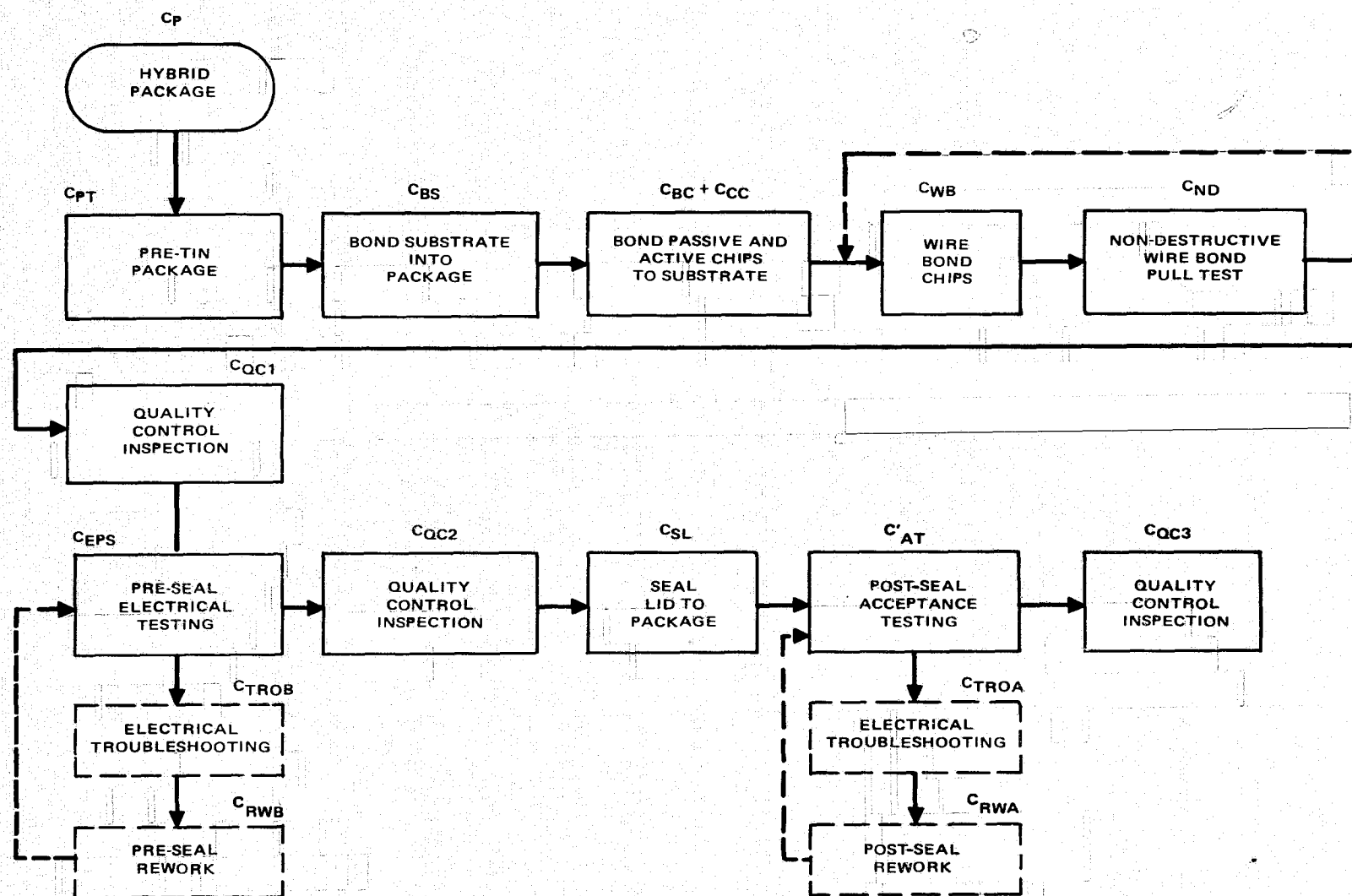


Figure 2-4. Hybrid microcircuit assembly and test

TABLE 2-4. NON-RECURRING DEVELOPMENTAL COSTS (p₁)

Cost Category	Cost Breakdown	Percentage of Total Developmental Cost	Developmental-To-Manufacturing-Cost Ratio	Eng. Material Cost As a Percentage of Each Cost Category
Engineering	Application Eng. 34%	54%	7.8	8.7%
	Design Layout 24%			
	Package Drawing 16%			
	Test Procedure & Fixture Design 16%			
	Burn-In Fixtures 5%			
Engineering Proof-of-Design Models	Planning for Continuation of Production 11%	36%	5.1	8.8%
	Eng/Production Support 7%			
	Total Fabrication/Assembly 51%			
	Total Test 31%			
Engineering Preproduction Models		10%	1.3	12%

TABLE 2-5. NON-RECURRING MANUFACTURING COSTS (p₂)

Cost Factors	Percentage of Total Non-Recurring Manufacturing Cost	Non-Recurring-to-Recurring Manufacturing Cost Ratio
Test Fixtures	35%	3.5
Masks	20%	
Screens	20%	
Burn-In Fixtures	15%	
Tooling	10%	

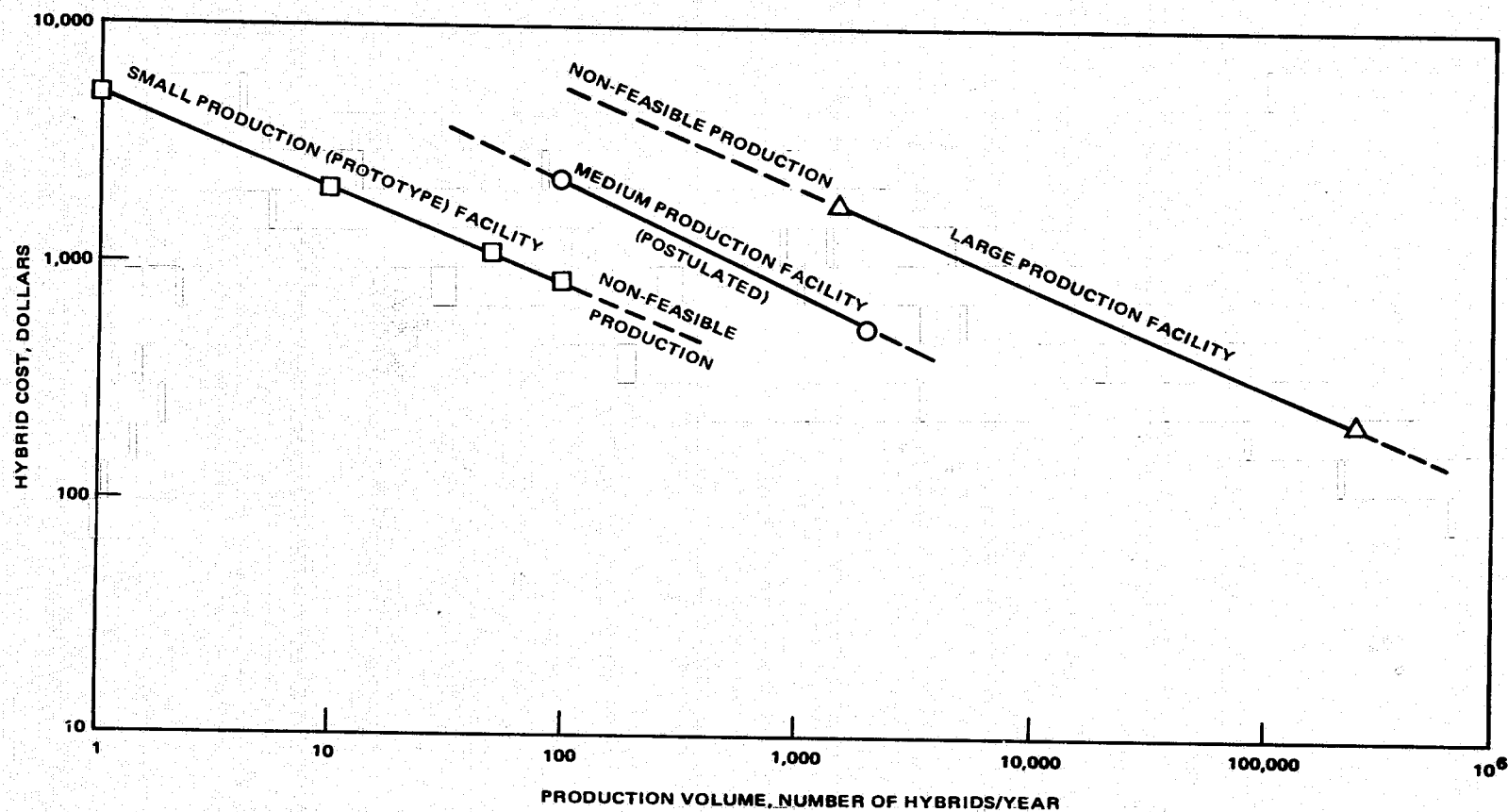


Figure 2-5. Hybrid cost as a function of production volume for different types of facilities

are related to the constants (γ_0), derived by the intersection of each curve with the cost axis, and reported in Table 2-6.

The total hybrid cost then is expressed in dollars by the equation:

$$\begin{aligned}
 C_H &= C_M + (C^0 S_P + C^0_{AT}) P (p_1, p_2, C_C) F(V) \\
 &= C_S + C_P + C_{CC} + C_L + (C^0_{SP} + C_{PT} + C_{BS} \\
 &\quad + C_{BC} + C_{WB} + C_{ND} + C_{QC1} + C_{EPS} + C_{TROB} + C_{RWB} \\
 &\quad + C_{QC2} + C_{SL} + C'_{AT} + C_{TROA} + C_{RWA} + C_{QC3} \\
 &\quad + C_O) W_R (p_1 + p_2 + 1) C_C (V)^{-B}.
 \end{aligned} \tag{5}$$

The "pre-seal electrical test" and the "troubleshooting before sealing" terms have been modified to include a factor η which accounts for the number of rework cycles. Therefore:

$$C_{EPS} = \eta g (\bar{N}_{TRJ})^{0.1} C_C \text{ for pre-seal electrical, and} \tag{6}$$

$$C_{TROB} = \eta' g' (\bar{N}_{TRJ})^{0.1} C_C \text{ for troubleshooting.} \tag{7}$$

(The meaning of each single term and the procedure used to derive them can be found in "Design, Processing and Testing of LSI Arrays-Hybrid Microelectronics Task, Final Report, NAS8-32607, September, 1978.)

TABLE 2-6. PRODUCTION FACILITY FACTOR (γ)

Production Volume	Intercept γ_0^{**}	Factor γ
Small	5,200	2.5
Medium	12,000	5.77
Large	33,000	15.86
* This coefficient is obtained by intercepting the curves of the cost-versus-volume graph (Figure 2-5) with the cost axis.		

The above cost equations have been applied in actual cases, and some formula modification was necessary to find the best fit for the experimental data. One major refinement of the formula was accomplished by reviewing the reference hybrid parameters (Table 2-7) so as to make proper adjustments for hybrid complexity. Adjustments made with respect to other parametric values are included in Tables 2-1 and 2-2.

2.1.2 Computer Programming and Models Verification

Computation of the cost function by computer (in standard hours, and without materials costs) was accomplished during this time period as an applications example. It was found that the models developed for hybrid microcircuits are easy to computerize, and that there is a large amount of information that can be obtained through computer analysis. The most

TABLE 2-7. REFERENCE HYBRID PARAMETERS

Hybrid Size	0.75" x 1.75"; Area = 1.3125 in ²	
Number of Package Leads	74 (only 60 actually are used)	
Number of Connections (Pads) per Chip	14	
Active Chip (Reference) SN 54LS138, Elmo Semiconductor Corp (TI)	40 Transistors (9 gates)	
Number of Hybrids Produced/Yr	1.2 x 10 ⁵	
<u>Components</u>	<u>Thin</u>	<u>Thick</u>
<u>Active Chips</u>		
Transistors and Diode (Area = 1/4 IC Area)	13	6
ICs (50 x 65 mils)	12	6
<u>Passive Devices</u>		
Capacitors (Area = (1.5 - 2.5) IC Area)	20	10
Resistors	30	10
Resistor Size (3K Ω)	0.0075" x 0.090"	0.04" x 0.075"
Space Taken by Active and Passive Devices (Including Resistors)*	50 - 70%	35 - 50%
(% of this Space Taken by Resistors	20%	35%)
Number of Bonds (Length of Bond = 50 Mils)	640	340
Overall Process Yield	95%	91%
* The remaining space is taken by the conductor network.		

impressive of these analyses can be performed by using computer graphics to visualize a "cost surface" in three dimensions. Cost surfaces can be generated for each couple of desired variables. The cost equation summarized in Appendix A and the program included in Appendix B were used to generate a matrix of cost values, which then was inputted to an in-house graphical display program. The resulting example of a cost surface is shown as Figure 2-6.

When a single output value of the cost function is desired (for a given set of input variables), the computer program reported in Appendix C can be used. The versatility of the computer programs developed under this contract are such that they can be utilized on any terminal attached to large computer systems in use at or available to many companies and/or Government agencies. This versatility is shown not only in the mathematical program foundation, which has been reduced to simple expressions, but also in the adaptability of these programs to real situations. Large computers not always are readily available; and in many cases, an analysis of the cost function does not always require the degree of sophistication which can be achieved by such a computer. A fairly accurate determination of the cost function may be performed rapidly by using a portable programmable calculator, such as the HP-19C; the associated program is included as Appendix D.

2.1.2.1 Modeling of Printed Wiring Board Fabrication

A first step in modelling the fabrication of a printed wiring board for single or multilayered structures involved the creation of a flow chart showing the processing sequence, with steps which are meaningful to the total fabrication cost. The actual process may be represented by a flow chart sequence, such as that reported in Figure 2-7. During the balance of the program, a mathematical model based on this flow chart will be created.

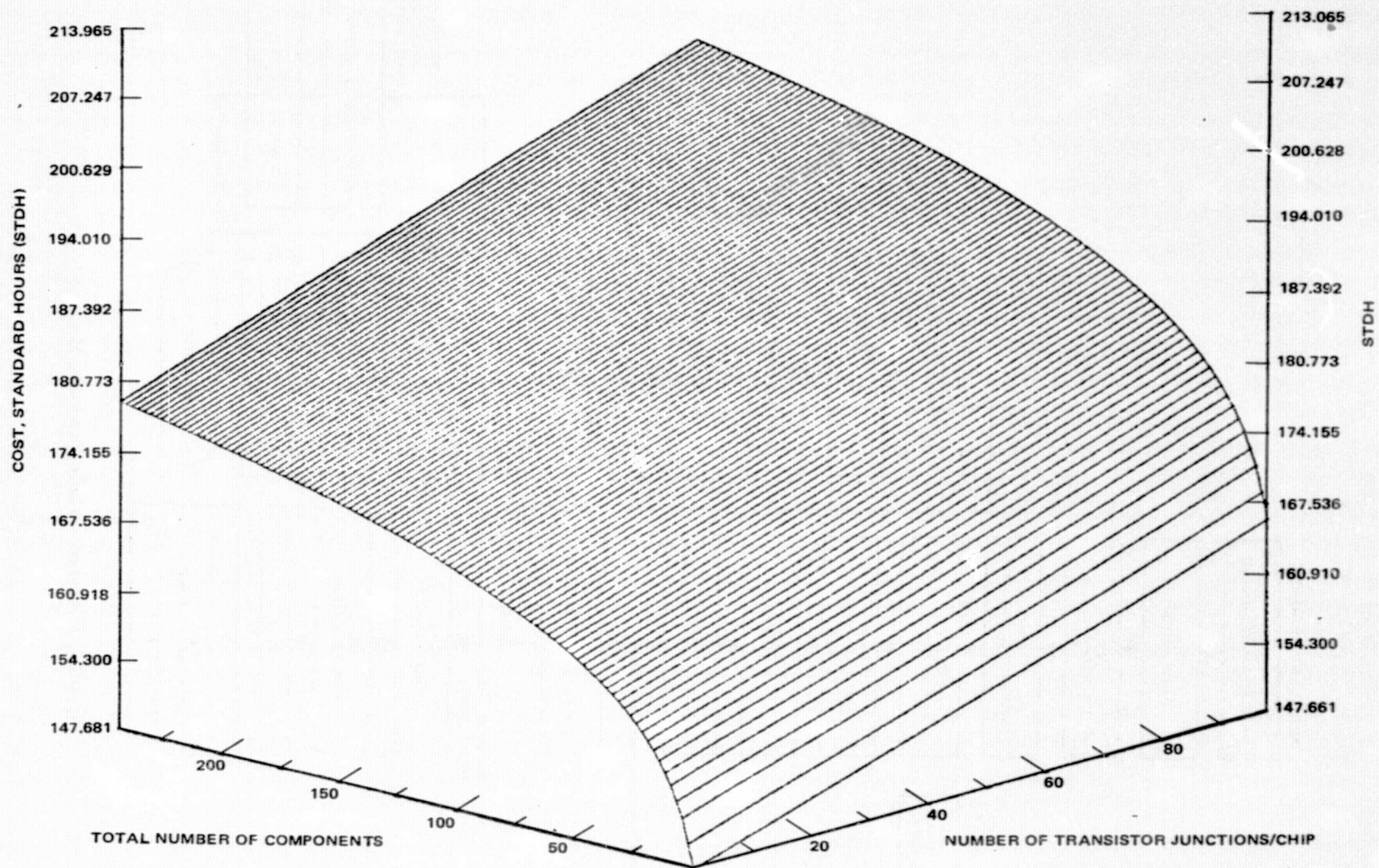


Figure 2-6. Cost surface of a hybrid microcircuit — front view

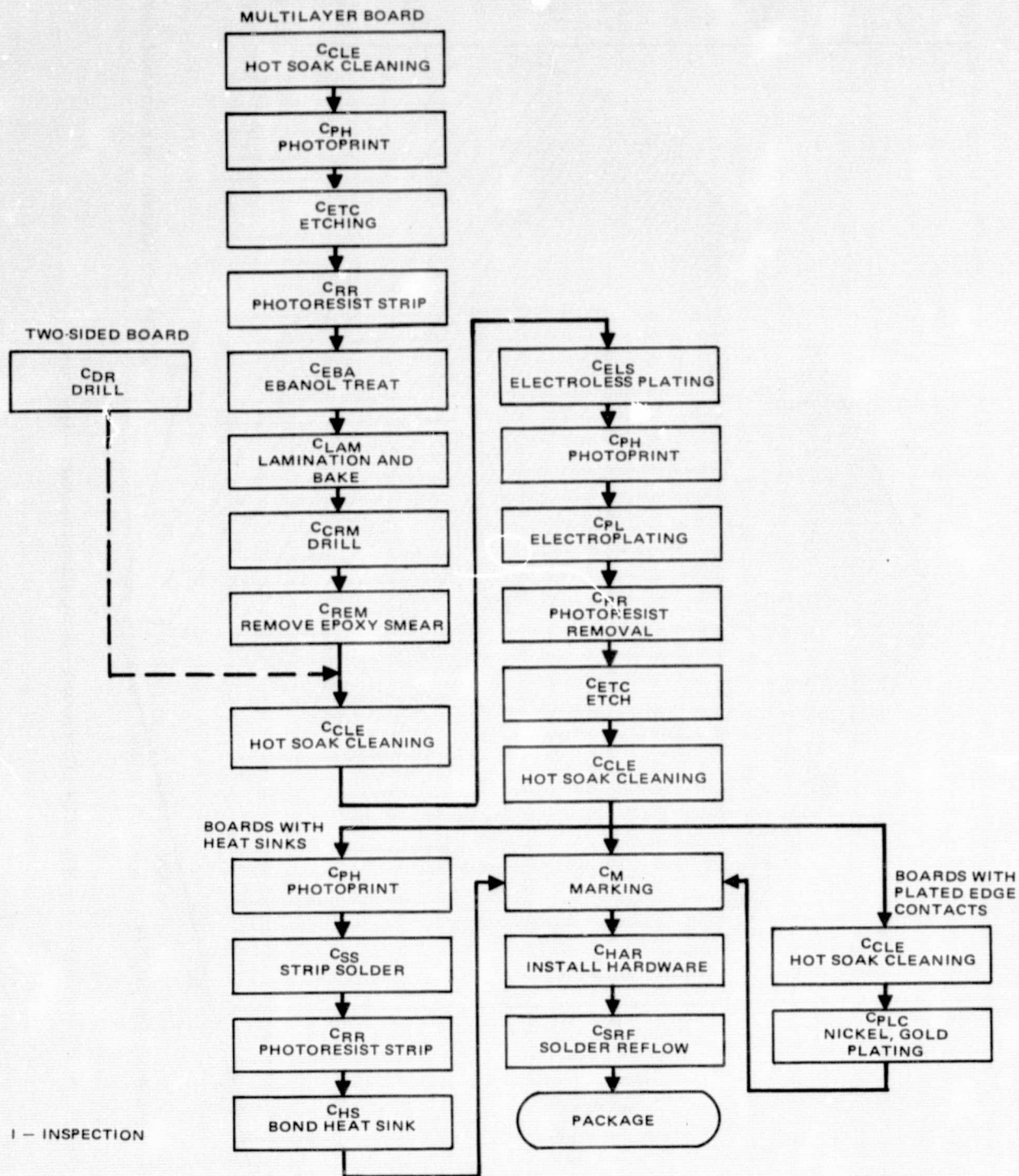


Figure 2-7. Printed wiring board processing sequence

2.2 TASK B - TAPE CHIP CARRIER (TCC) DEVELOPMENT

Yield improvement has been the main thrust of emphasis under Task B during the past six months. Processes were examined closely, and problem areas have been identified so that appropriate corrective action could be taken. This approach resulted in improved photofabrication and handling techniques; related to both tape and wafer processing. Out of these efforts also grew an invention which now is being prepared for disclosure and possible filing with the United States Patent Office.

2.2.1 Tape Process Refinement

In tape fabrication, liquid photoresist is applied to the copper side of the film, exposed through a tape photomask, and developed. In previously-used methods, a dry film photoresist was laminated to the window side of the tape just prior to etching, to prevent etching loss of copper from the backside, and to provide mechanical support to the lead fingers formed by the etching operation. This dry film resist on the backside, as opposed to liquid resist, performs well for the purposes intended, providing lead support during processing which is far more effective than that provided by liquid resist. In addition, this material is relatively easy to remove after etching and prior to plating. A problem with lead etching was identified when it was noted that the leads were reduced significantly in thickness and width in the areas immediately overhanging the window edges. This over-etch situation increased lead fragility, which resulted in undesired lead bending during subsequent operations. Such bending often caused a loss in the critical registration required for inner-lead bonding to the chip. It became apparent that such lateral movement of the leads prior to bonding could be catastrophic.

The cause of this problem of course is the "tent" effect which results from the gap created when the 1.8-mil-thick dry resist film is applied over the five-mil step between the back polyimide film surface and the back surface of the copper laminate.

The dry film photoresist, originally designed for printed wiring board fabrication, does not provide good coverage in holes or in the recesses of steps, as in the case with copper laminated over punched polyimide tape.

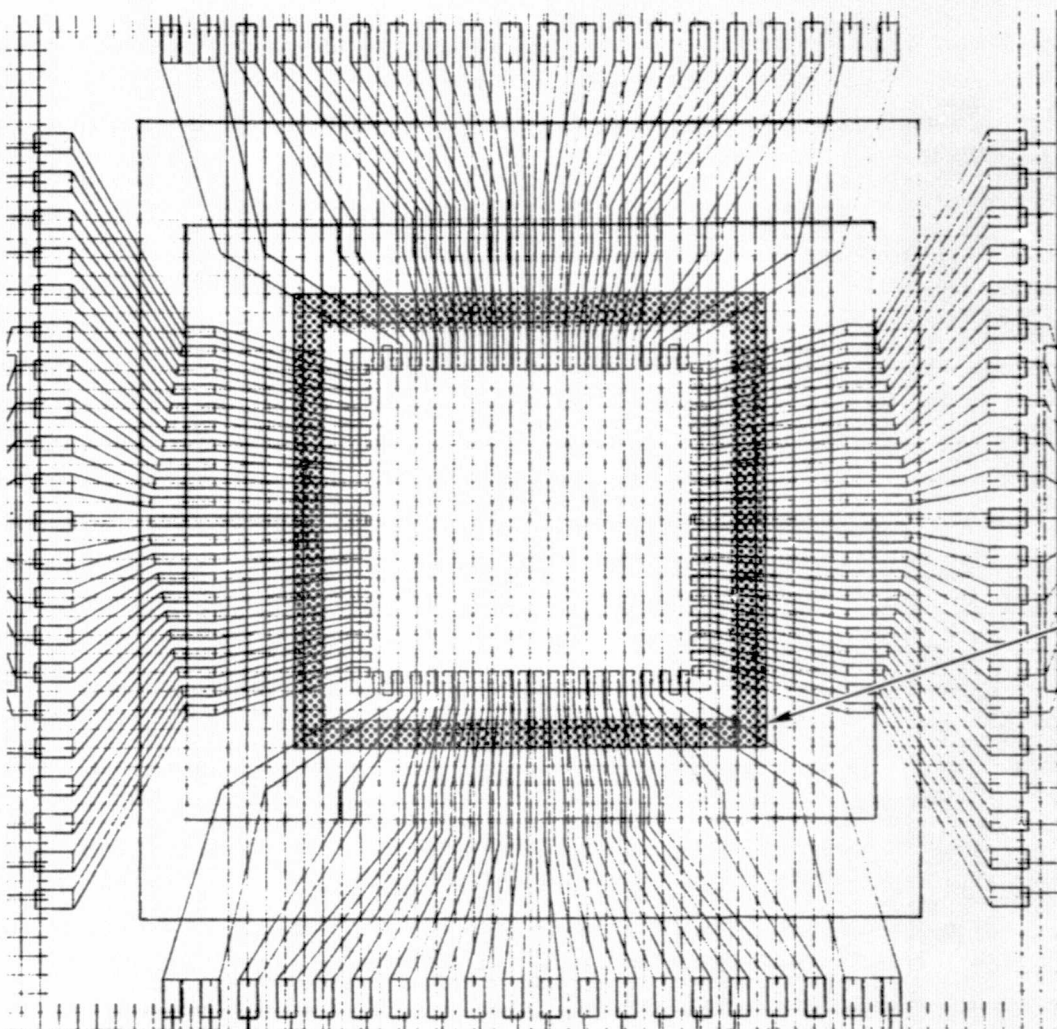
Consequently, bare copper on the backside of each etched lead was unprotected from the etchant, which then caused the noted reduction in lead thickness and width. The problem was solved by coating this stepped area with liquid photoresist prior to laminating the entire backside with dry photoresist, thus preventing unwanted etching behind leads near the tape window edges, while still providing the required lead support during etching. Utilizing Riston D2000 Stripper, both the dry and liquid photoresist are removed together after etching.

This procedure has been incorporated as a part of the standard tape processing procedure at Hughes, and the over-etch problem has not recurred.

2.2.1.1 Removable Lead Support

Window size and lead density are increased when tape chip carrier processing is applied to larger chips. This has the effect of increasing the lead length-to-width ratio, bringing about a direct impact on processing yields. The fragile leads (generally 0.003 in. to 0.005 in. wide and 0.0014 in. thick at the inner ends) fabricated through copper etching can overhang the film windows by 100 mils or more, and they easily may become damaged during processing so that registration to the chip pads is lost. A support ring such as that illustrated in Figure 2-8, rigidly attached between the inner- and outer-lead bond sites during tape fabrication, would minimize such damage. This ring can be made as an integral part of the tape by selectively punching the window to leave a polyimide ring before laminating with copper. Special tooling for the tape punching is required for this ring style, and additional supports (shown in Figure 2-9) are required to support the ring prior to the copper/polyimide laminating process. These additional supports can interfere with the excising and outer-lead-bonding (OLB) processes, unless specialized tooling is made to excise or bond around them. After excising and OLB, the polyimide ring material cannot be removed -- it remains a permanent part of the packaging scheme. This approach therefore may be used only where organic materials are permitted within the package itself.

A ring that easily is removable after outer-lead bonding urgently is needed for lead support within military/space-grade hybrid microcircuit packages, where usage of organic materials cannot be tolerated. This



ECL 82-PAD
PATTERN
SHOWING
"DOUGHNUT"
PLACEMENT

Figure 2-8. Support-ring concept

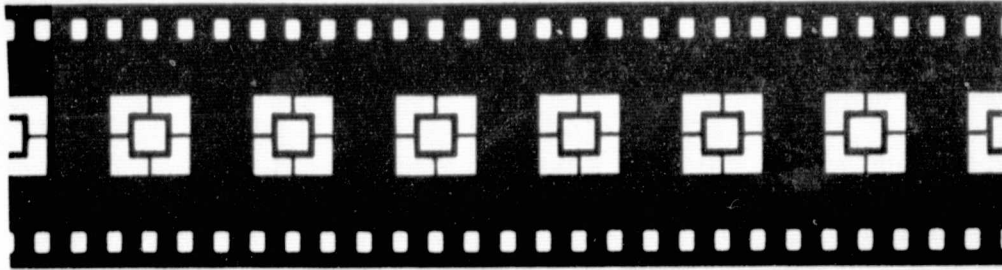


Figure 2-9. Polyimide support ring formed by special tape punching tools.

requirement has spurred the search for a method of producing a support ring which does not require expensive special tooling, and which subsequently is easily removable without damaging or contaminating the bonded units. The choice of processing method and materials also must be such as to permit the relatively high temperatures associated with inner- and outer-lead bonding.

This search has led Hughes to investigate the processing of photo-sensitive materials that can be defined by standard photolithographic techniques without special tooling, and can be removed by means of conventional stripping operations. Initial work, detailed below, represents reduction to practice, and the idea soon will be disclosed and submitted to the United States Patent Office.

An ECL high-speed, high-power LSI device (a MUX chip) was used as a demonstration vehicle for this investigation. This 0.180-inch-by-0.190-inch chip contains 82 bonding pads, and typically is mounted in a custom-made chip carrier as shown in Figure 2-10. The support ring for this unit was

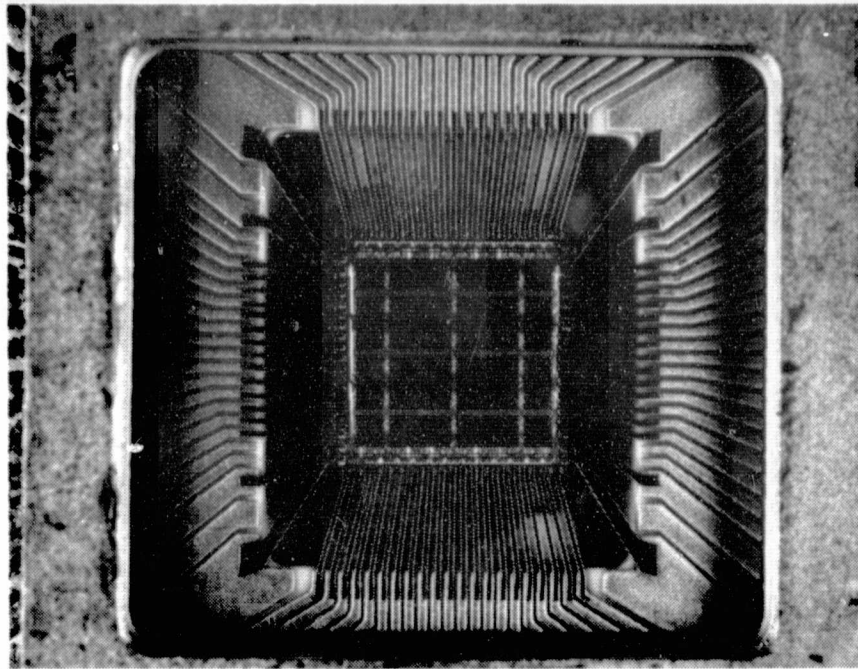


Figure 2-10. 82-pad ECL device mounted in hermetic chip carrier
via TCC processing

made 0.015 in. wide, and was located 0.015 in. from the chip edges to permit proper mechanical support without causing interference with the inner- or outer-lead bonding operations. Registration of a support ring on the window-side of the tape was a natural extension of previous work at Hughes involving the lamination of dry film resist for this purpose (Paragraph 2.2.1 above).

As shown in the flow chart of Figure 2-11, tape fabrication starts with application of liquid photoresist on the copper side, followed by exposure and development of the lead pattern. The window-side then is laminated with dry film resist as discussed earlier; but in this case, the resist is left unexposed to UV light up to and including the copper etching operation. In this way, lead support is maintained, and protection from backside etching is assured. This dry-film resist subsequently is exposed through a special support ring photomask, after which it is developed to remove the resist from all areas except for the desired ring on the bottomside of the leads. Dry film resist development also removes residual from the wet resist located on the copper side of the tape.

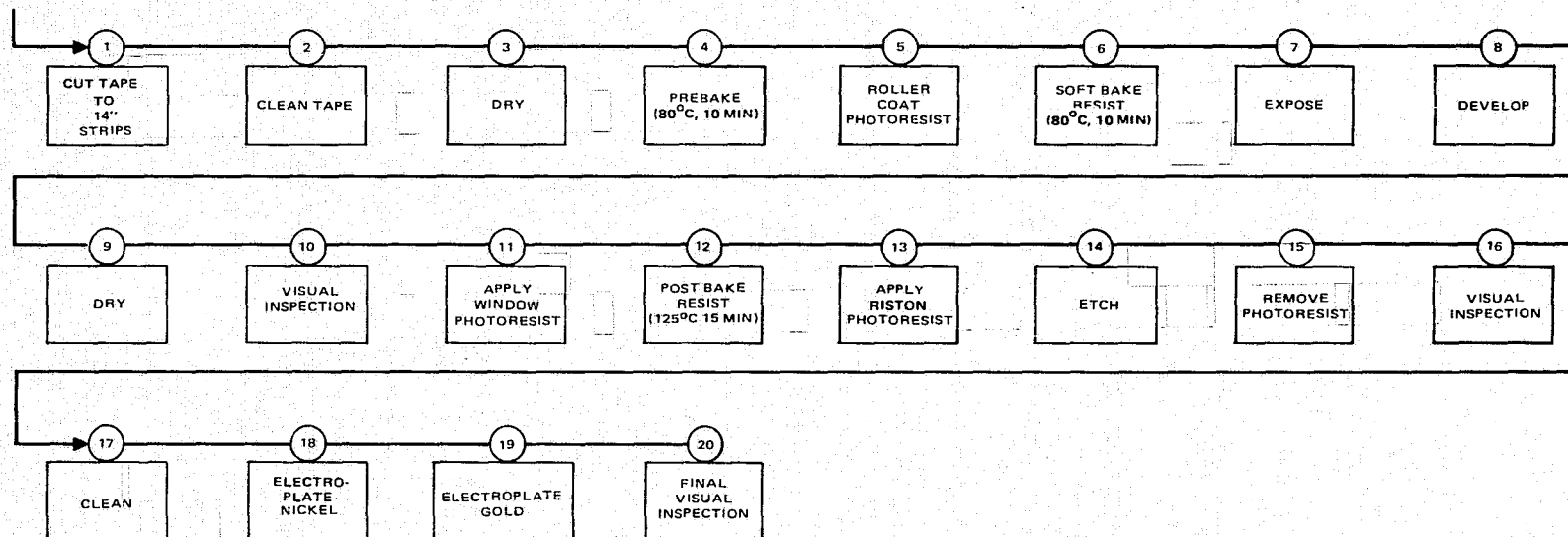


Figure 2-11. Tape processing flow chart.

The support ring then remains on the tape throughout all plating and bonding operations to prevent damage and possible pad-registration problems. It may be removed by means of a plasma photoresist stripping operation prior to final sealing.

Initial process feasibility has been established by using Riston Type 218R (a duPont dry film photoresist) as the support ring material. Work is continuing to substitute a DuPont solder mask material (Type 730FR) for the Riston. This new material is expected to provide the same support and protection afforded by the Riston 218R, while increasing the potential for resisting thermal stresses encountered during bonding operations.

2.2.1.2 Processing Increased Film Lengths

During initial tape fabrication efforts (1978 program), tape lengths were limited to three inches. The raw material (punched polyimide laminated to one-ounce copper) was supplied as a continuous length, which subsequently was cut to smaller lengths for adaptation to existing photoresist equipment; i. e., equipment normally used for processing of three-inch-diameter wafers or 2-inch x 3-inch ceramic thin film resistor-conductor networks. With 35 mm film (ANSI Standard), there are four bond sites in each three-inch strip; after processing, these often are reduced to two or three sites through yield loss, or to permit electrical contact at tape ends during electroplating operations.

Recognizing the need to process longer strips of tape for increased yields, Hughes developed improved photoresist and handling procedures during this time period. These procedures first were developed for strips of seven inches in length, and as handling improved, the strip length involved has been increased to 12 inches. Some work has been performed with 18-inch tape lengths, where additional leader is needed for use with the inner-lead bonder (paragraph 2.2.3). The actual usable bond area for both the 12-inch and 18-inch lengths of tape is 11 inches (14 potential bond sites). This 11-inch length represents maximum capacity of the Hughes-fabricated photoresist exposure unit (Figure 2-12) currently being used, but this length capability can be increased with additional equipment modifications.

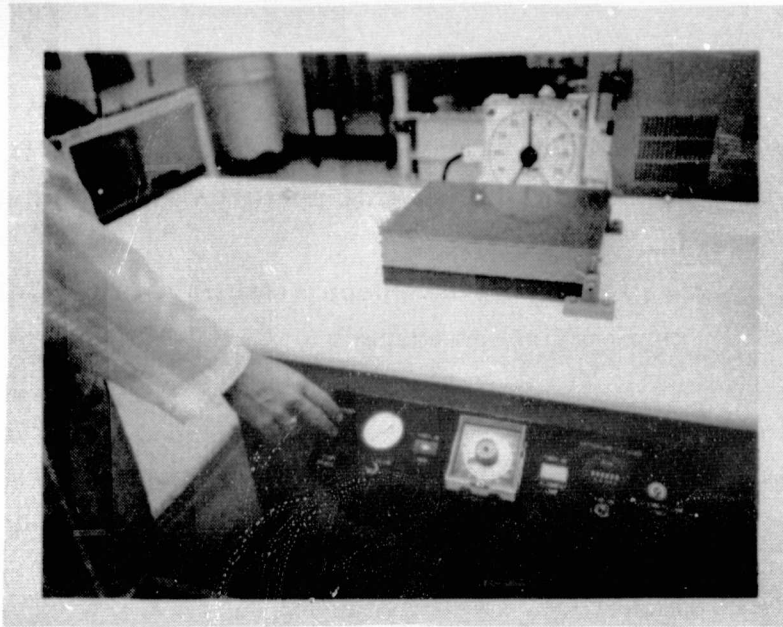


Figure 2-12. Hughes-fabricated photo resist exposure unit.

One of the first processing changes required to permit usage of longer tape involves the method of coating copper with liquid photoresist. Spin coating was used originally (1978 program), but this approach became impossible when the length was increased beyond three inches. Dip coating was considered, but this was not attempted because it leads to potential problems caused by uneven photoresist thicknesses. Roller coating with a Gyrex Type 9 Microcoater (Figure 2-13) was evaluated for this application. Good results were obtained, and this technique has been adopted for applying liquid photoresist to tape carriers.

Etching the longer tape was not a problem, since a Chemcut Model 547 Spray Etcher (shown in Report No. P78-549, Figure 2-10, page 2-40) currently is being used. This etcher will be capable of handling a continuous length of tape when suitable feed and take-up reels are added. Developing and stripping operations, now being performed in trays, will be switched over to vertical tanks within the next three months. This change will bring about improved control and better space utilization. Deeper electroplating tanks also will be used in this time period to accommodate a new plating rack for the tapes. This plating rack, shown in Figure 2-14, is capable of plating six 12-inch lengths of tape simultaneously. It was designed by

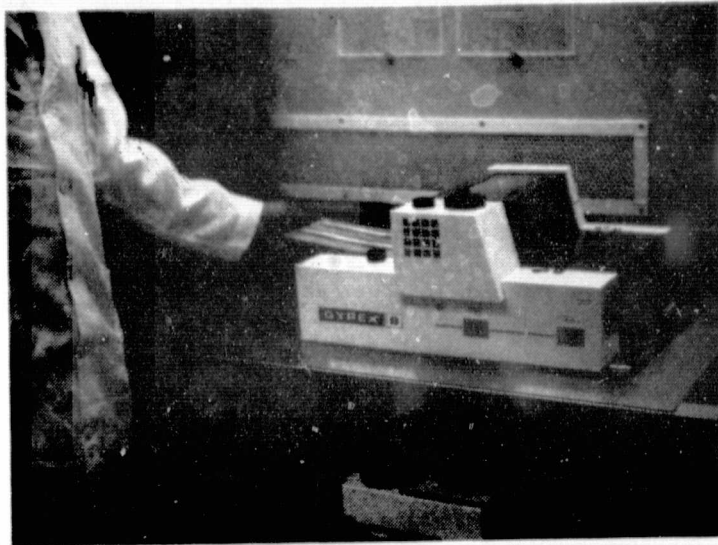


Figure 2-13. Gyrex Type 9 microcoater.

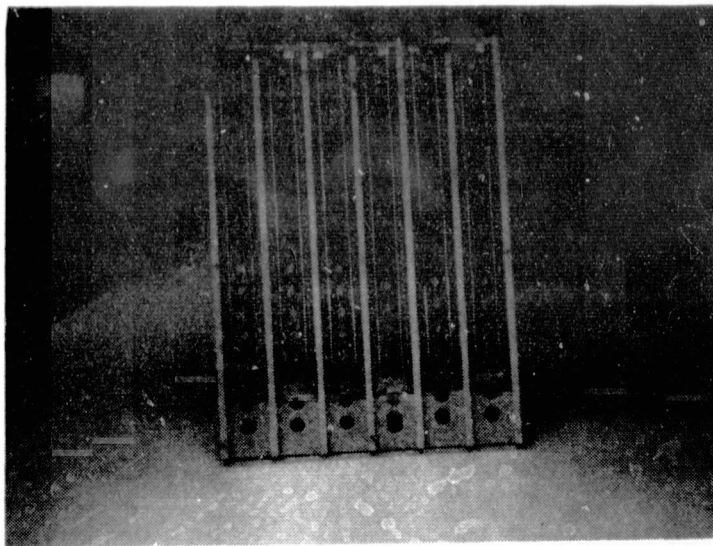


Figure 2-14. Plating rack designed originally by Honeywell/
St. Petersburg, Florida (U.S. Army ERADCOM Contract
No. DAAB07-77-C-0526).

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

Honeywell/St. Petersburg, Florida, in connection with their TCC Manufacturing Methods and Technology Program (U.S. Army ERADCOM Contract No. DAAB07-77-C-0526). The holes located in the plastic cover over each chip bonding site permit increased electrolyte circulation, and consequently increased gold plating thickness where needed, while reducing plating thickness (and saving gold) in other areas.

2.2.2 Wafer Bump Process Refinements

In the conventional method of plating gold bumps on semiconductor wafers, the wafers are oriented vertically in the plating solution, and a single electrical contact is made at the top of each wafer. Agitation of the solution is from the bottom of the plating tank, and this usually results in a non-uniform flow of electrolyte across the surface. Such a deposit results in a varying bump thickness. Non-uniform bump height can have a negative effect on inner-lead bonding (ILB) yield; it therefore becomes necessary to minimize this height-variation problem.

One approach toward solving the bump-uniformity problem recently has been introduced within the tape chip carrier industry. This approach involves orientation of each wafer in a horizontal position, with the surface to be plated facing downward; thus bringing the electrolyte solution to the wafer via a vertical fountain-type holder, as illustrated in the diagram of Figure 2-15. Methods such as this produce more uniform flow of plating solution than is possible with the conventional approach, and the result is a more uniform deposit of gold bumps on the wafers.

Arrangements were made to evaluate the fountain concept initially through an outside source. A three-inch-diameter wafer supplied by Hughes was metallized, prepared with dry film photoresist, and shipped to the vendor for bump plating. The deposition results were satisfactory, and it was decided to fabricate a working system in-house.

Parts for this system have been received, and equipment fabrication will be completed during the next reporting period. Fountain-type plating equipment is available commercially from a Japanese supplier (Fuji Advanced Corporation) through its North American and European distributor, IMI, Inc.,

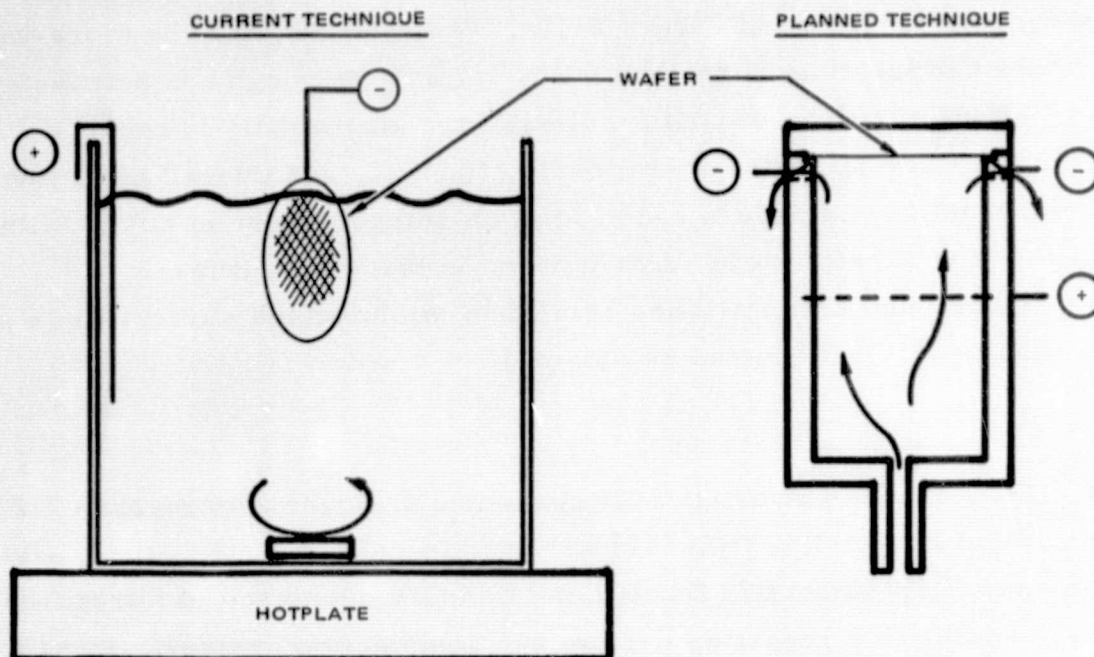


Figure 2-15. Vertical and horizontal wafer plating concepts

Cherry Hills, New Jersey. The cost of this equipment is higher than ordinarily might be expected, because it has been designed to include timed variable-voltage power supply increments during plating, so that the bumps can be grown through spun-on wet photoresist (0.0002 inch to 0.0005 inch thick), rather than through the 0.0018 inch-thick dry photoresist preferred by Hughes. Use of the former results in shorter "mushroom-shaped" bumps, as their height rises above the relatively thin resist layer. The latter approach (dry resist) produces more satisfactory bump shapes; particularly when adjacent bumps are located closer than 0.005-inch apart. In addition, the in-house-designed-and-fabricated fountain-plating equipment will permit closer control of processing parameters.

2.2.3 ILB Process Refinement

Previously-reported ILB studies (Paragraph 2.2.3, page 2-50 of Report No. P78-549) were conducted by utilizing modified K&S Model 675 Beam Lead Bonders. During this reporting period, Hughes received a Model 207 production-grade Inner-Lead Bonder, purchased from International Micro Industries (IMI), Cherry Hill, New Jersey as a capital equipment item.

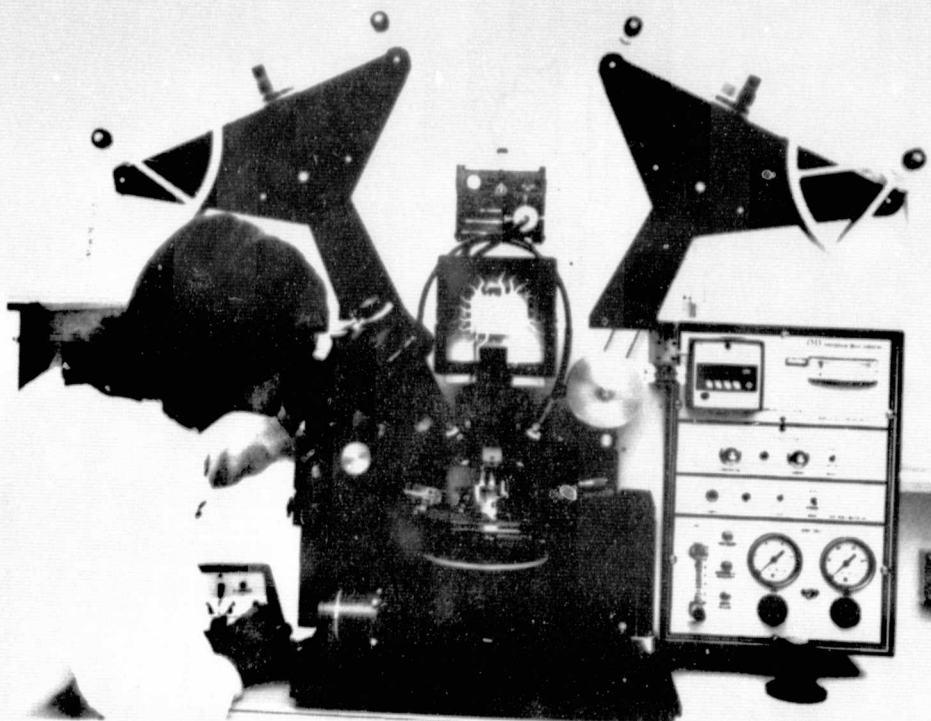
This equipment, shown in Figure 2-16a, was selected over the more-widely-used Jade Corporation inner-lead bonder after a thorough competitive evaluation involving relative versatility, flexibility, adaptability to hybrid microcircuit applications, operational reliability, and overall effectiveness. The close-up view of Figure 2-16b shows a bumped wafer in place, with the matching tape carrier strip superimposed in the film carriage.

Initial checkout activities related to this machine currently are underway; results will be reported as obtained.

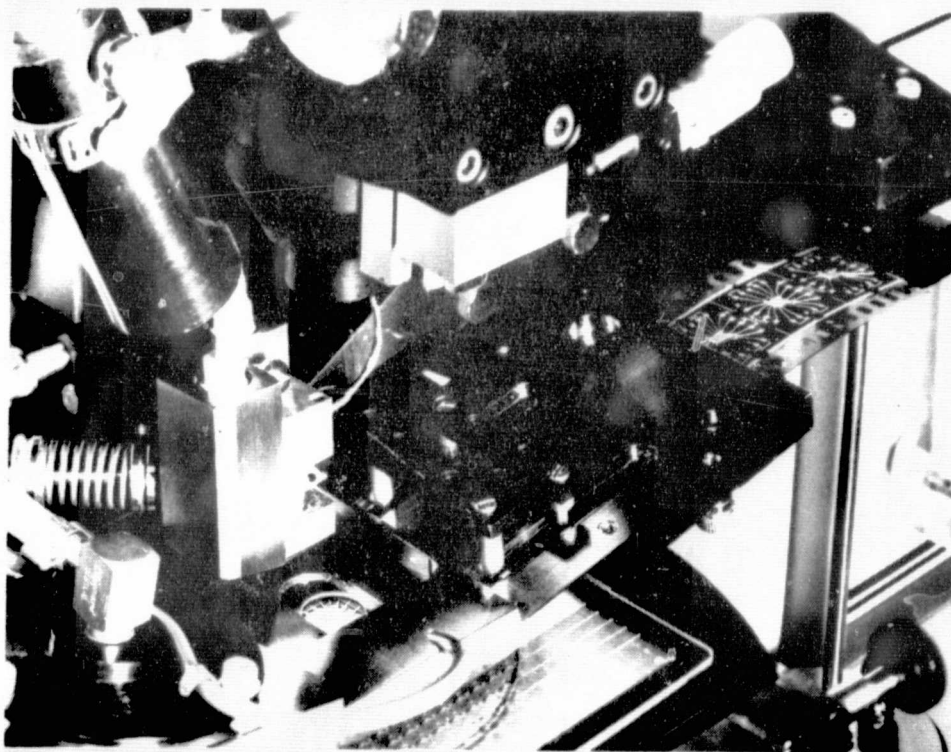
2.2.4 OLB Process Refinement

OLB process investigations conducted at Hughes (Paragraph 2.2.4, page 2.54 of Report No. P78-549) utilized specially-adapted collets attached to the same K&S Model 675 Beam Lead Bonders discussed in Paragraph 2.2.3 above. During this reporting period, the combination excise/forming tool diagrammed in Figure 2-17 was designed and ordered through the Hughes Industrial Products Division (IPD), Carlsbad, California. An assembly drawing of this tool (delivery of which is expected during July, 1979) is shown in Figure 2-18.

Hughes has procured a manual Outer-Lead Bonder from IPD. This bonder, shown in Figure 2-19, may be used in either a pulse-reflow-solder or a thermocompression-bonding mode. It utilizes a Hughes thermocouple-controlled AC power supply and a Hughes welding head fitted with a tungsten-carbide square-ring bonding tool. The unit is designed to supply a controlled "Time-At-Temperature" heating pulse with separate time, temperature, and force adjustments. Its operation, shown in the close-up of photograph of Figure 2-20, involves vacuum pick-up of the "spider" (excised chip with formed tape-carrier leads attached); placement of the substrate (in this case represented by the hermetic chip carrier) through light-beam alignment; and outer-lead bonding by foot-pedal action: as the foot pedal is depressed, the vacuum quill and surrounding collet is lowered until the "spider" die makes contact with the substrate, on which an appropriately-located "dot" of epoxy has been placed. As the pedal is depressed further, the collet makes contact around the OLB lead periphery, and sufficient pressure is applied to activate the digitally-timed power supply, either in a pulse-reflow-solder or



a) OVERALL VIEW



b) CLOSE-UP OPERATING VIEW

Figure 2-16. IMI Mode 207 inner-lead bonder

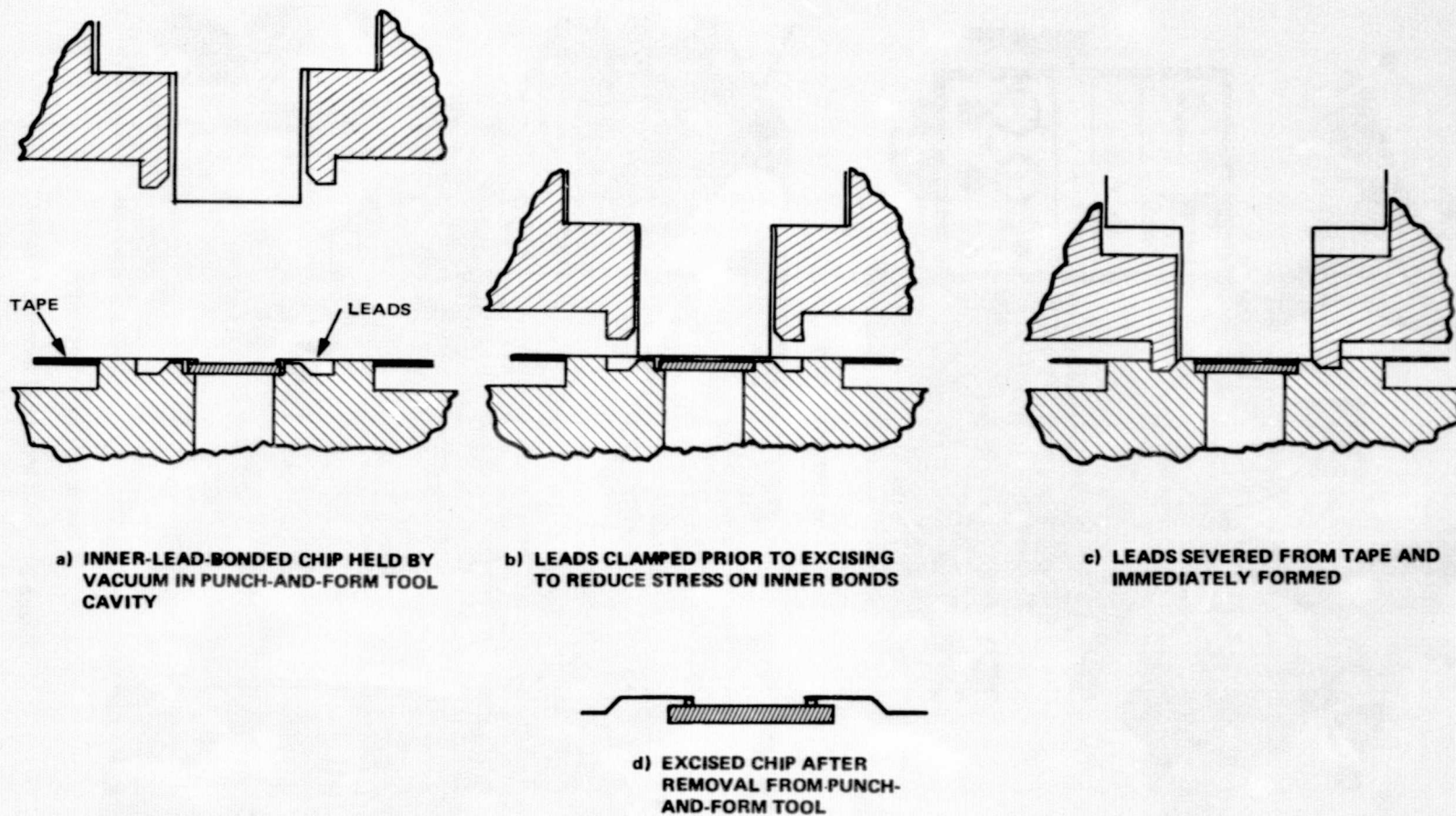


Figure 2-17. Combination excise/forming tool operation diagram

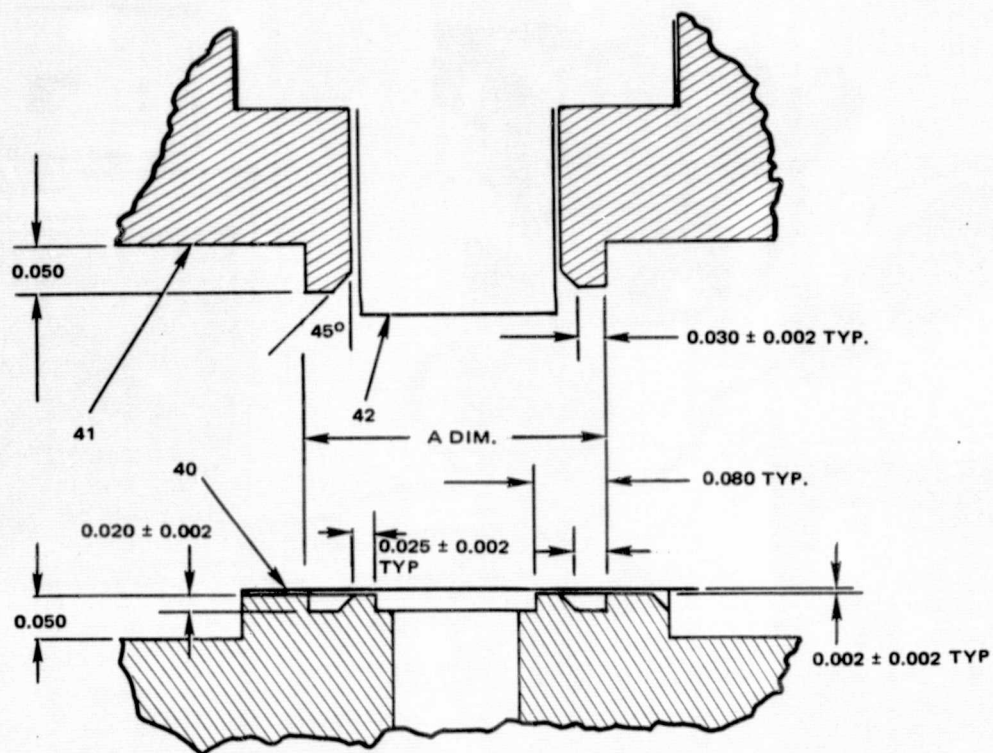


Figure 2-18. Combination excise/forming tool-assembly drawing

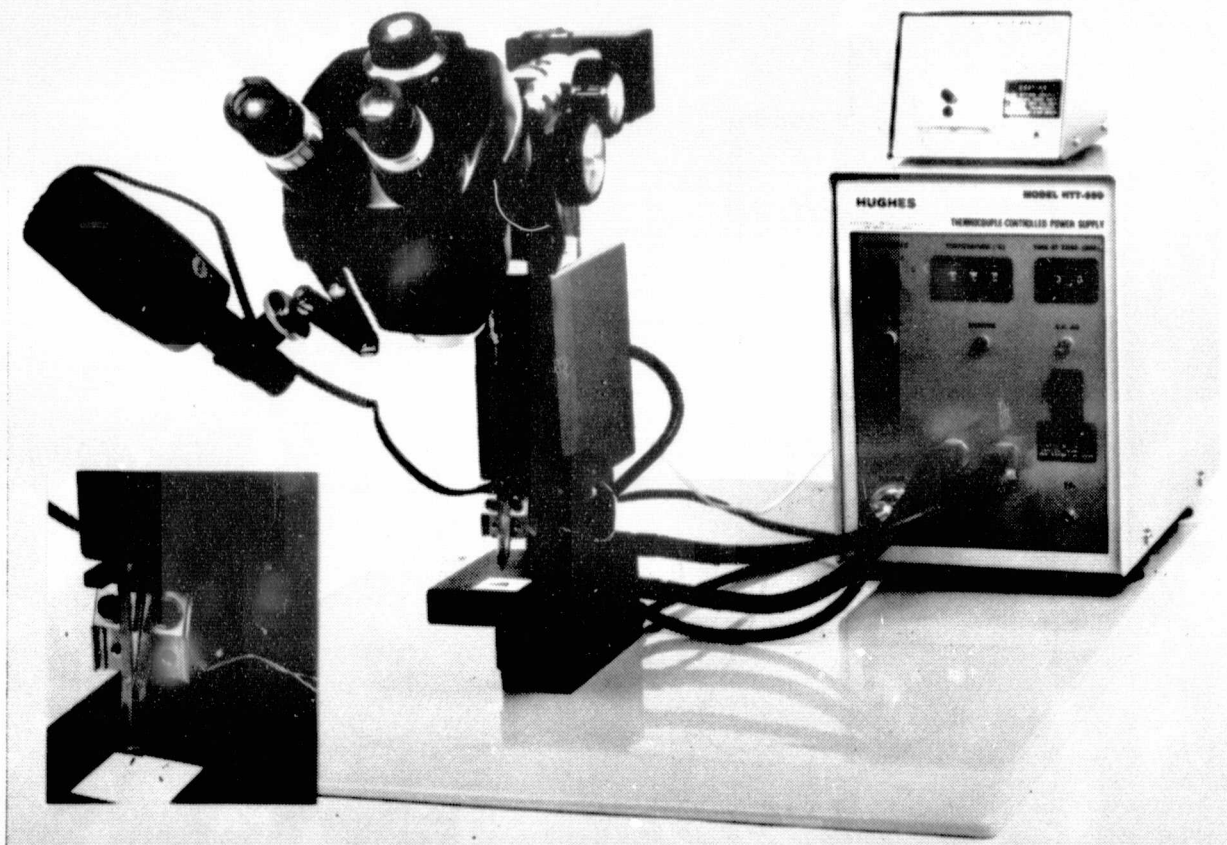


Figure 2-19. Hughes-IPD manual outer-lead bonder

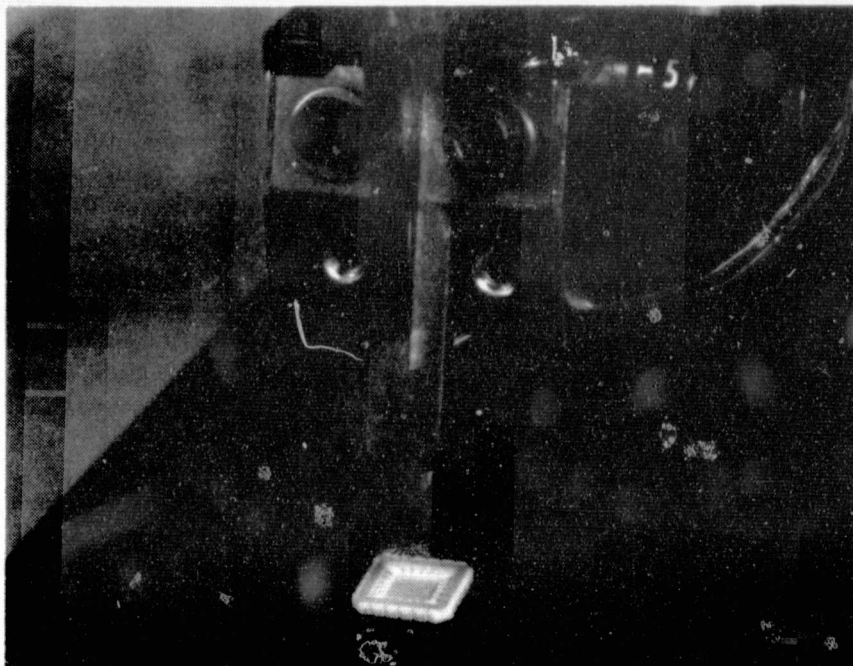


Figure 2-20. Close-up operation of Hughes-IPD manual outer-lead bonder

thermocompression bonding mode. After pre-set heat and pressure is applied to make the bond, the preprogrammed power supply turns off, and cooling action takes place. At this time, the pedal is released, and the next "spider" assembly may be aligned for vacuum pick-up. A typical outer-lead-bond to a thin film gold metallization pattern requires a tool temperature of 450°C , pulsed for one second at 17,000 psi per bump. Stage heating need not be used in this outer-lead bonding process.

This OLB concept readily will be adaptable to semi-automatic operation when capital funding becomes available. Hughes OLB activities currently are confined to those which can be accomplished with the manual unit. Appropriate tools have been ordered to demonstrate OLB processing of the semiconductor devices listed as A, B, C, and D in Table 1-1. The remaining OLB tools (including those required to demonstrate TCC processing of STAR devices) will be procured as the need arises for their use.

2.2.4.1 Pull-Test Results with Chips Mounted in Hermetic Chip Carriers

Hughes Type HCMP 1824 wafers (32 x 8 Static RAMS) were bumped, inner-lead-bonded, excised, and outer-lead-bonded to standard 24-lead commercial-style hermetic chip carriers to form pull test samples. The bumped wafers exhibited a 75-to-90 gram bump shear strength with all failures occurring as chip-outs in the silicon beneath each bump.

The size of the chip is 0.117 in. x 0.156 in., leaving a lead span of 70 to 105 mils within the chip carrier. Lead widths at inner ends varied from 4.0 to 4.5 mils. Double-bond pull testing was performed at a rate of four grams-per-second, with the hook gripping in the center of the span. The mean pull strength of 122 leads was 53.2 grams, with a standard deviation of 12.6 grams (n-1 weighting). A histogram of the data is shown in Figure 2-21. A majority of the pull strength failures occurred in the lead itself, with only one bond lifting from the chip carrier pad at 45.6 grams. Other modes of failure included lifting at the inner bond, bump shearing at the thin film interface, and chipping of the silicon beneath the bump.

2.2.5 Test/Burn-In Process Refinement

All tape designs for semiconductor devices (listed in Table 1-1) utilized as investigative vehicles under this program include provisions for burn-in and functional testing after ILB, as discussed in Paragraph 2.2.5, page 2-54 of Report No. P78-549. The manual punch-out tools shown in Figure 2-22a and 2-22b are used to remove tape metallization shorts, and appropriate wire bonds are added where required. An example of the TCC tape punch-out sequence and resulting interconnections for plating, burn-in testing, and functional testing required for a typical CMOS device, is shown in Table 2-8 and illustrated in Figure 2-23. During the next reporting period, after ILB operations for this LSI device have been completed, burn-in/functional testing will be demonstrated by utilizing these interconnection arrangements.

2.2.6 Hybrid Microcircuit Applications

A Hughes-designed Digital Correlator Hybrid Microcircuit (Part No. 1040568) used on an advanced-technology Air Force communications

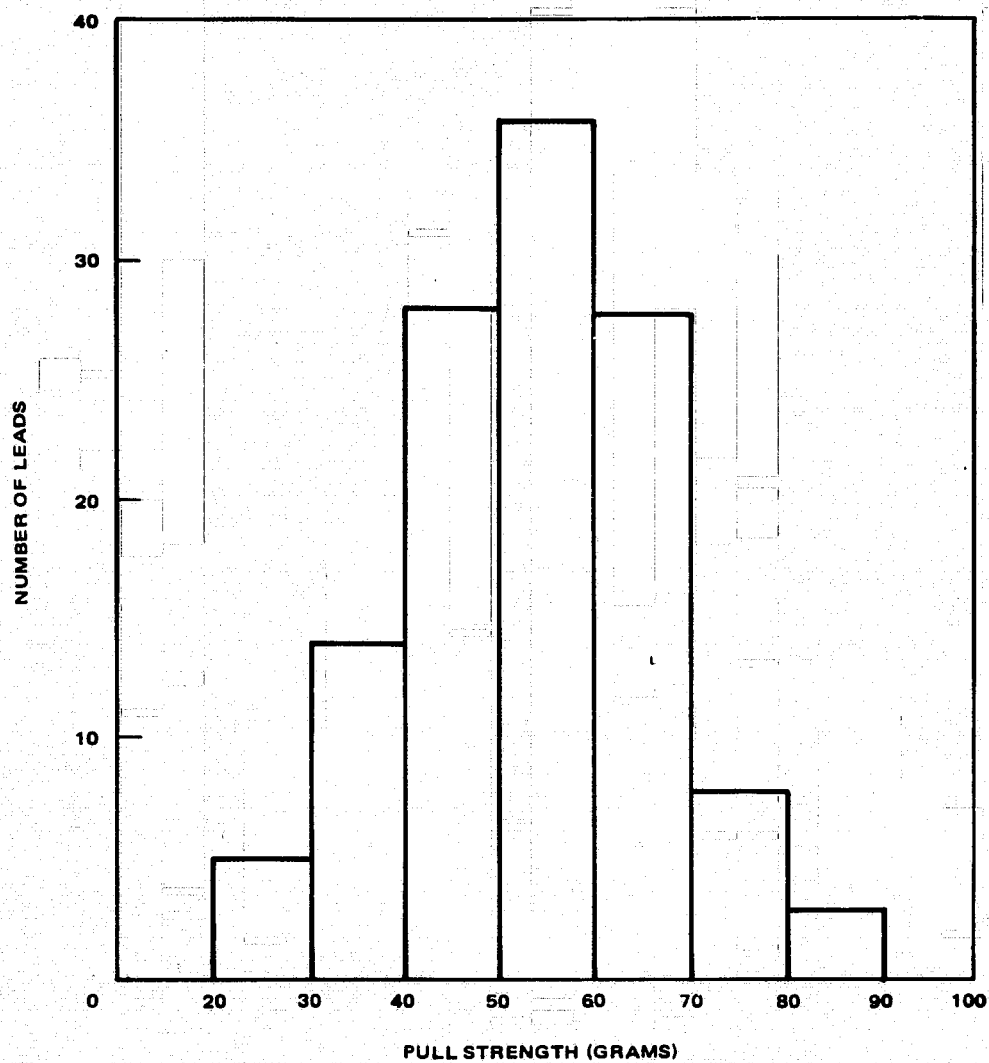
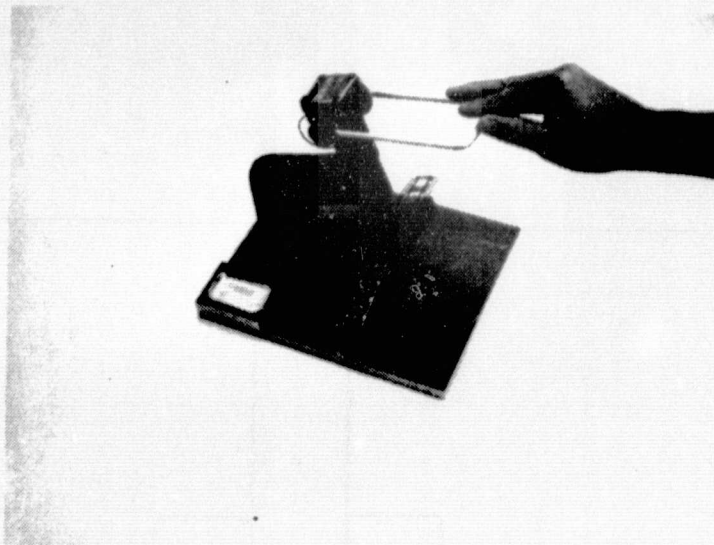
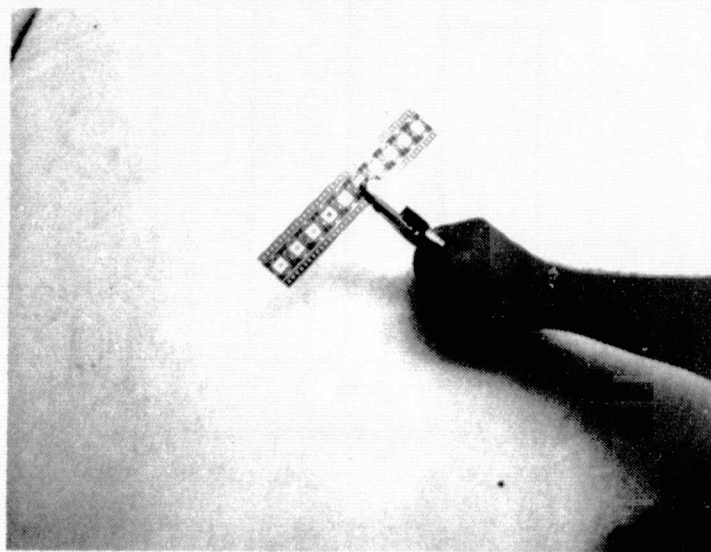


Figure 2-21. Double-bond pull test distribution — 1824 static ram in 24-pad HCC package



a) TOOL/DIE PUNCH-OUT SET – BENCH-TOP MOUNTING

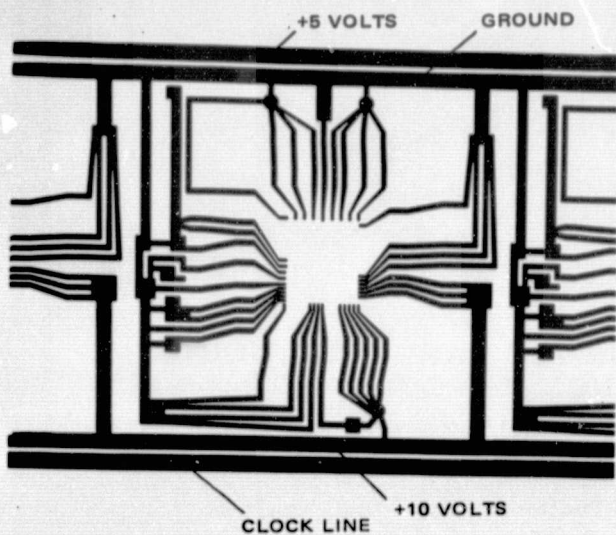


b) HAND-OPERATED PUNCH-OUT TOOL

Figure 2-22. Manual punch-out tools

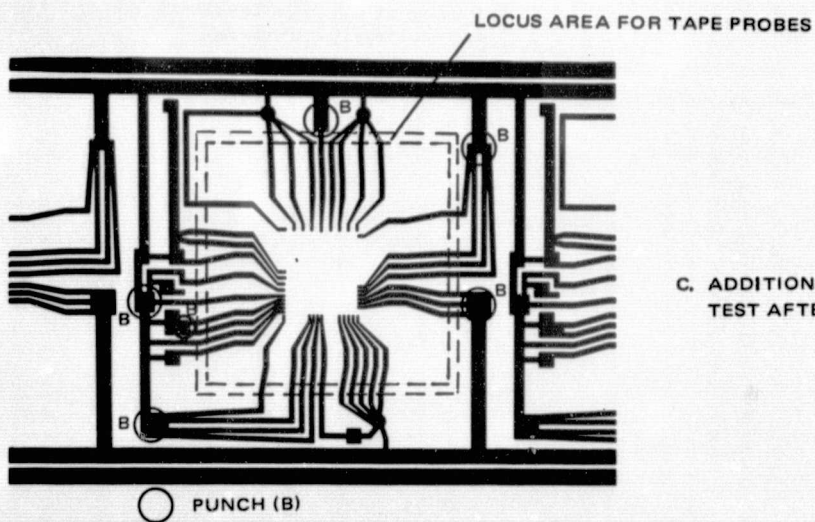
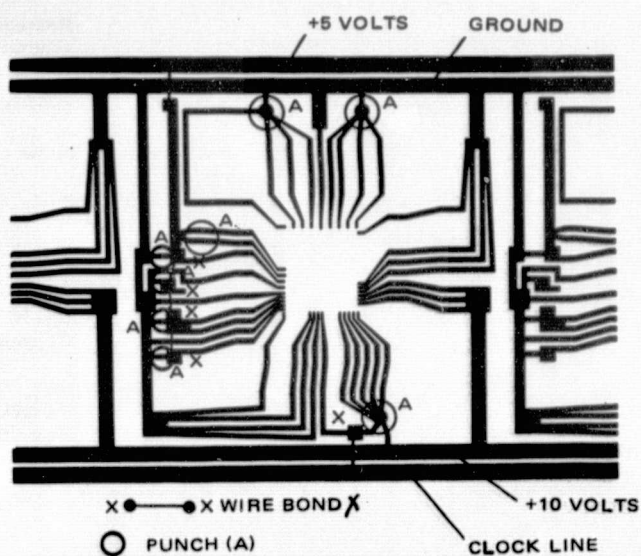
TABLE 2-8. EXAMPLE OF TCC TAPE PUNCH-OUT
CONNECTION SEQUENCE (TYPE 342 CMOS
DIGITAL CORRELATOR)

<u>Condition No.</u>	<u>Description</u>	<u>Pattern Punch- Out and Wire- Bond Connections</u>	<u>Remarks</u>
1.	Original Tape Pattern (Figure 2-23a)	None	All metallization electrically interconnected to permit electrolytic gold plating
2.	Burn-in Tape Pattern (Figure 2-23b)	Positions "A" Punched Out. Wire Bonds "X-X" Connected.	Interconnections remain for burn-in testing. <u>Bias Voltages:</u> 5 volts from outside bar to ground; 10 volts from inside bar to ground.
3.	Functional Test Tape Pattern (Figure 2-23c)	Positions "B" Punched Out. All Wire Bonds Broken.	Probe Pins apply a +5-volt signal between pad 3 and ground (pads 4, 13, 23, and 34); a -5-volt signal between pad 24 and ground; and a +10-volt signal between pads 1/2/20/21/22 and ground. Functional test outputs appear as specific levels at appropriately-numbered clock and signal pads.



A. PLATING INTERCONNECTIONS

B. PREPARATION FOR BURN-IN



C. ADDITIONAL PREPARATION FOR FUNCTIONAL TEST AFTER BURN-IN.

REMOVE WIRE BONDS (X - X of FIGURE 2-23B)

Figure 2-23. A plating interconnections

system has been selected for the first TCC process demonstration circuit under this program. As shown in the schematic diagram of Figure 2-24, this microcircuit is an excellent example to illustrate the economic need for TCC technology, since a single relatively complex CMOS LSI device (Hughes Type 342) is utilized ten times. The conventionally-wire-bonded version, shown in Figure 2-25, currently is being fabricated in the Hughes-Newport Beach SSPD Hybrid Microcircuit Laboratory. First-pass yield rates typically are less than 50 percent, since the chips cannot be characterized functionally in a cost-effective manner prior to microcircuit assembly.

Mechanically-satisfactory Type 342 wafers have been bumped during this reporting period, as illustrated in Figures 2-26a and 2-26b. The patterned tape for this application is shown in Figure 2-27; this same tape is shown superimposed over the matching bumped wafer in Figure 2-28.

The single-layer thin film interconnection network (substrate) currently being utilized (Figure 2-25) will be replaced by an equivalent multilayer thick film network; the two metallization patterns and the dielectric pattern for this network are shown in Figure 2-29.

During the next reporting period, ILB operations will be completed; thick film multilayer networks will be screened/fired; and chip/lead "spider" assemblies will be excised and outer-lead bonded to illustrate the TCC version mechanically. Electrically-operating versions then will be fabricated, and comparative yields between the TCC and wired versions will be evaluated as permitted by program time and current funding levels.

2.2.7 STAR Wafer Application

During November, 1978 telephone conversations, cognizant MSFC personnel agreed to supply mechanical wafers and pad location masks so that Hughes wafer bumping activities on STAR devices could be initiated.

For the initial baseline concept, it was envisioned that 84-pad hermetic chip carriers (HCCs) would be used. The layout drawing of this HCC package (Figure 2-30) shows a 0.470-inch square cavity; initial HCC orders may specify a reduced cavity area of 0.270-inch x 0.270-inch to minimize wire bond lead length.

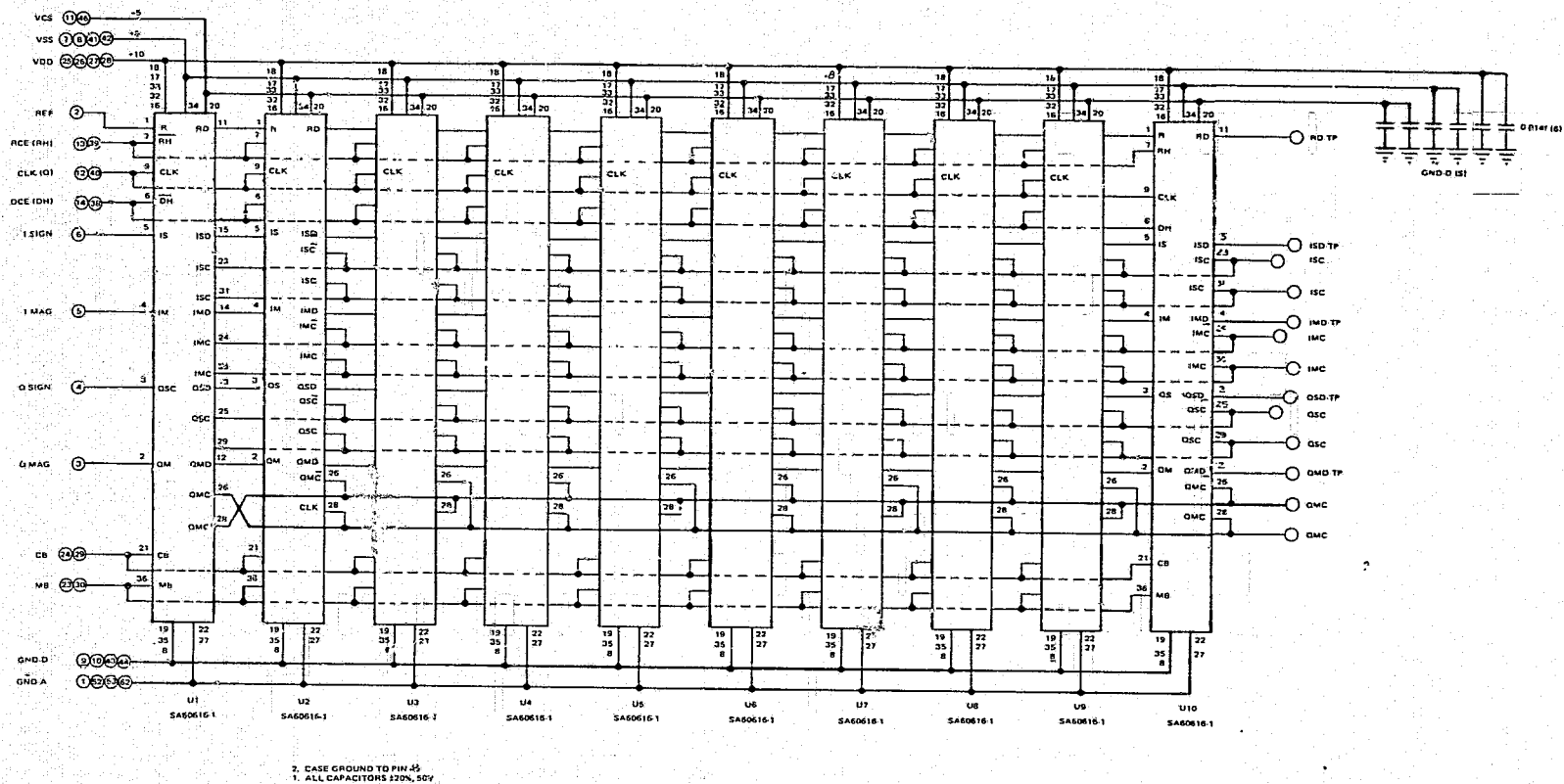


Figure 2-24. Schematic diagram of type 1040568 digital correlator microcircuit

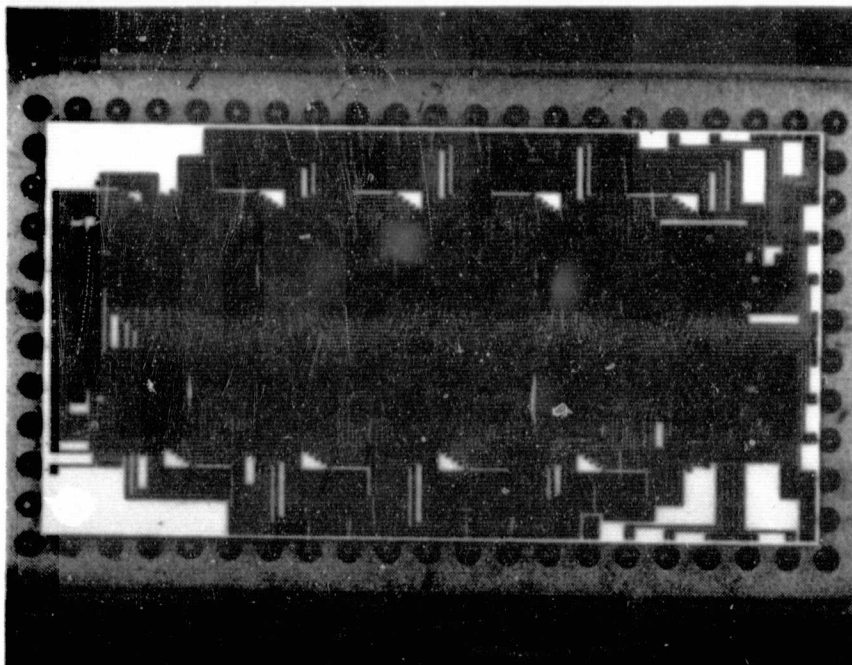
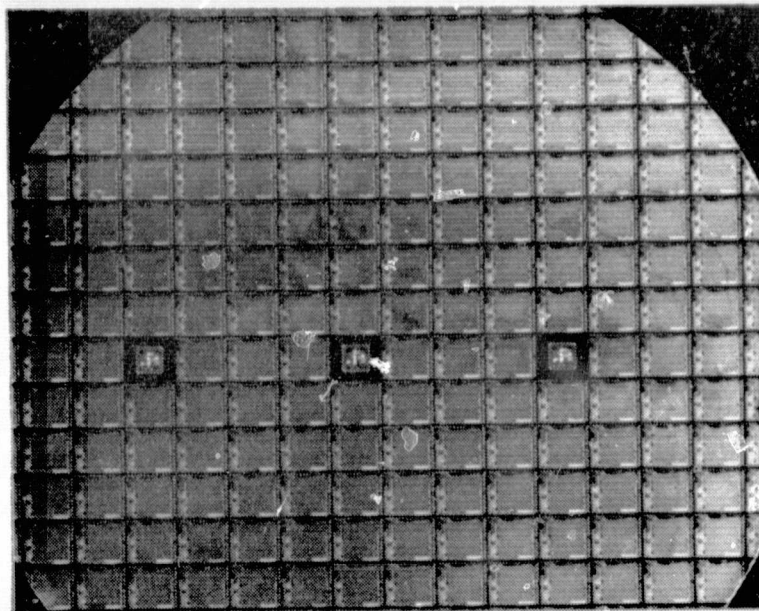
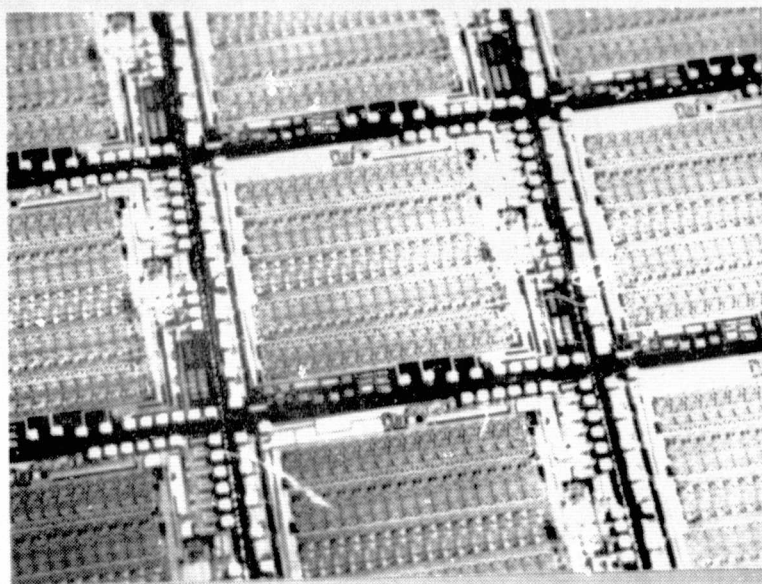


Figure 2-25. Conventionally wire-bonded version of type 1040568 Digital Correlator microcircuit

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR



a) FULL-WAFER VIEW



b) CLOSE-UP VIEW

Figure 2-26. Bumped type 342 CMOS digital correlator wafer

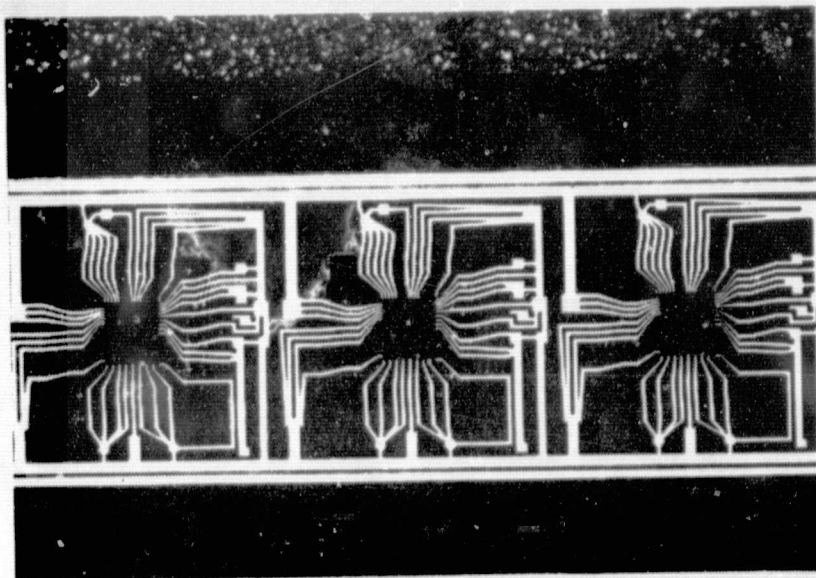


Figure 2-27. Tape carrier patterned for type 342 LSI devices

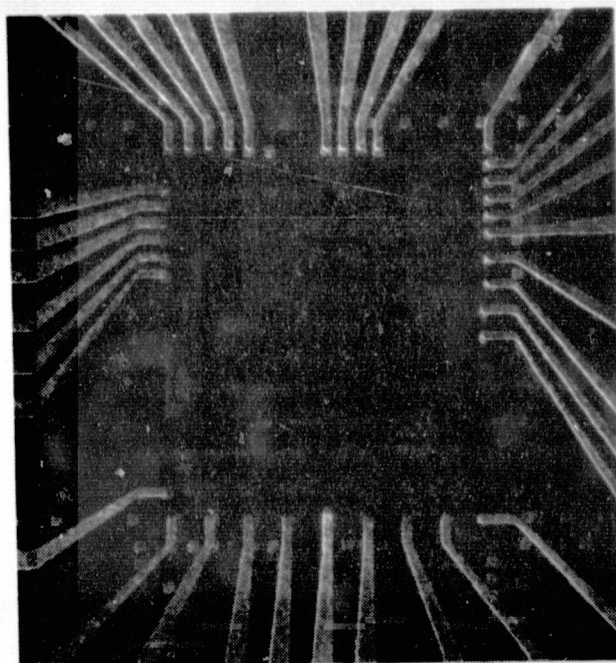
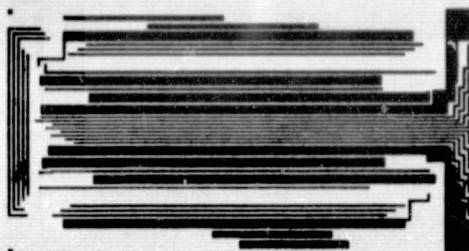
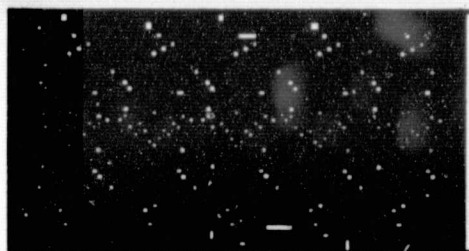


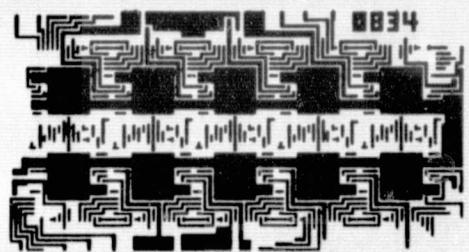
Figure 2-28. Tape carrier for type 342 devices shown superimposed over matching bumped wafer



FIRST CONDUCTOR



DIELECTRIC



SECOND CONDUCTOR

Figure 2-29. Metallization/dielectric patterns for type 1040568 digital correlator multilayer thick film interconnection network

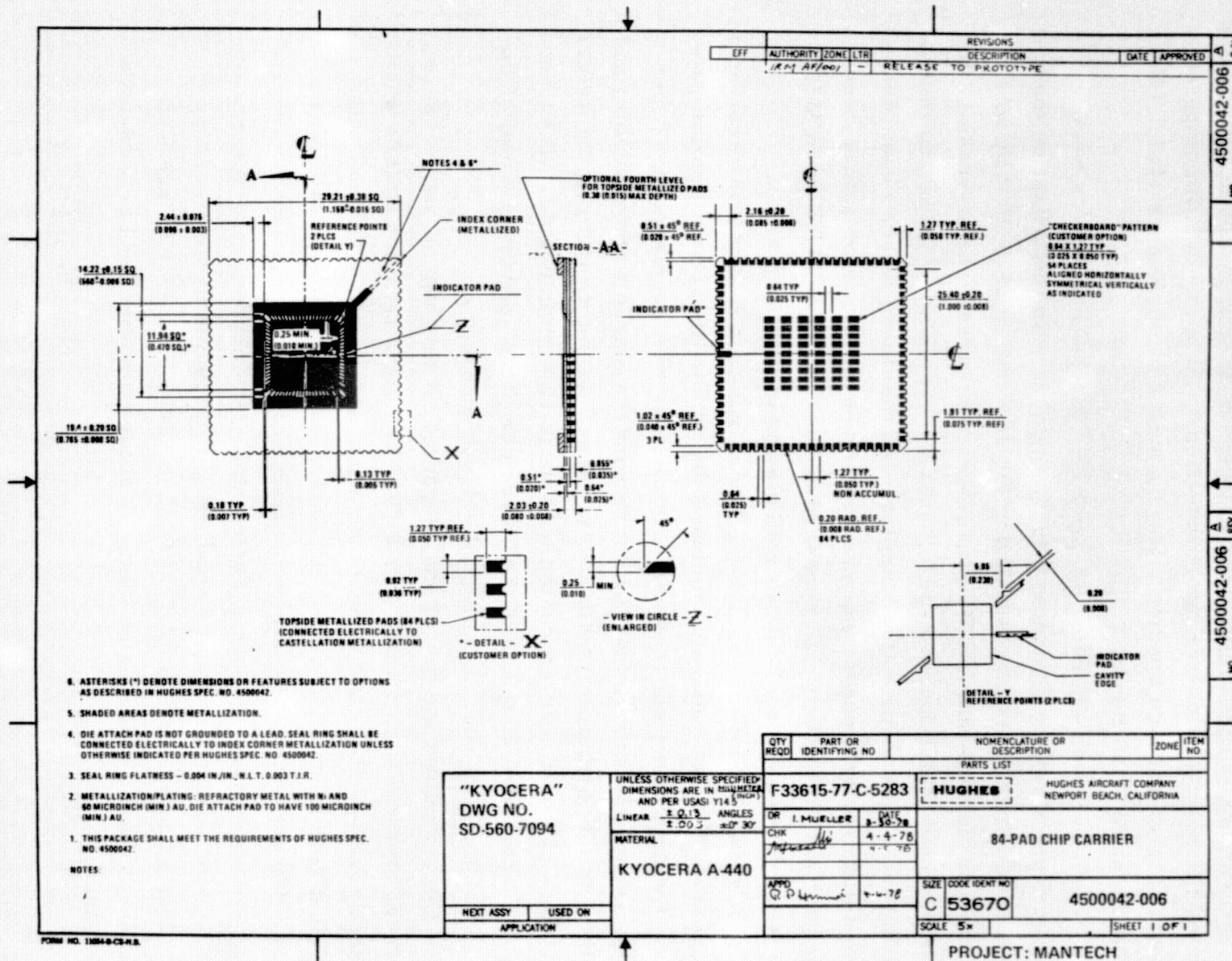


Figure 2-30. Outline drawing of 84-pad HCC package (Hughes Type 4500042-006).

Gold-bumped STAR devices will be bonded eutectically within the HCC package cavity (using either gold-silicon or gold-germanium preforms), after which one-mil gold wire interconnections will be made (both chip-to-chip and chip-to-package bonding shelf) by means of the Hughes Model 1460 Semi-Automatic Wire Bonder.

Eight 1.5-inch-diameter 38-pad STAR mechanical wafers were received from MFSC on 12 January 1979, together with metallization masks on 2-inch x 2-inch glass plates. During the 16 January 1979 visit by MSFC personnel to Hughes-Newport Beach, program progress was discussed. It was pointed out that 3-inch x 3-inch masks are required to match currently-used Hughes aligners for wafer bumping, and that these masks should include pad metallization locations/sizes only; the scribe lines and/or actual interconnection metallization which appeared on the masks received from MSFC were to be deleted to avoid excess gold plating in unwanted areas.

A second shipment comprising 3-inch x 3-inch masks was received on 22 January 1979, but these also included the scribe lines/metallization patterns. During subsequent telephone conferences with cognizant MSFC personnel, it was determined that the correct masks indeed were available; and that they would be shipped within several days. In the meantime, the wafers themselves had been sputter-coated with tungsten-titanium/gold. They were to be dry-resist-laminated, and then placed on "hold" pending receipt of the proper bump plating masks, expected early in February.

Corrected pad masks for the 38-pad STAR mechanical wafers were received from MSFC on 5 February 1979. The eight 1.5-inch wafers which had been received from MSFC on 12 January, and coated at Hughes with tungsten-titanium/gold, developed micro-cracks, and some actually were broken. Others broke after dry-resist lamination; a process which generally does not cause wafer breakage. The eight-to-ten-mil nominal thickness of these 1.5-inch-diameter wafers apparently contributes to their relative brittleness in comparison to the 2-1/4-inch, 3-inch, and/or 4-inch wafers normally subjected to the wafer bumping process (nominally 12-to-20-mils in thickness).

Attempts were made to align larger wafer portions, so as to yield initial bumped chips. This proved to be impractical however, and additional wafers were requested from MSFC.

When more wafers are received, they will be coated with tungsten-titanium/gold. Extra precautions in handling and transportation will be exercised to prevent reoccurrence of breakage.

After gold-bumping, the wafers will be sawed (using processing discussed in Report No. P78-549, Paragraph 2.2.2, page 2-43), and individual chips will be bonded eutectically within the 84-pad hermetic chip carrier as discussed above. Thermosonically-bonded one-mil gold wire will form interconnections between chips, and between the chips and package. The gold bumps on the chips will permit monometallic (gold-to-gold) interconnection bonding, and thus will eliminate the possibility of gold-aluminum intermetallic formation and associated problems. An electrical test of the wafer after bumping and before assembly is not planned at this time. In the past, this test was performed to detect etching damage to the aluminum bond pad metallization incurred during the bumping process. This still is a major concern during processing, but laboratory and design precautions have eliminated this problem, which has not occurred since initial process development.

Wafer dicing and assembly will take place immediately after the bumping process, so that testing may be performed at the package level. If tests reveal that bump contacts are suspect, the test previously-conducted after bumping will be resumed to trace the source of failure.

Periodic technical discussions are being held in an effort to plan the exact processing technology which will be followed to accomplish functional testing of individual STAR devices at the wafer level (after bumping, mounting, and sawing).

APPENDIX A

COST EQUATION SUMMARY

The equation used in the computer program is a simplification of the cost equation (5). This equation, when applied to a prototype facility, takes the form:

$$C_H = \{ 2.3 + 5.54 \times 10^{-3} \delta_R + 9.3 \times 10^{-3} N_C + 0.004 N_{WB} \\ + 0.34 C_C + (\eta 0.95 + 1.38) C_C (\bar{N}_{TRJ})^{0.1} \\ + \eta' 0.025 (g_1 + g_2) \} 12 C_C^{2.5} V^{-0.4}$$

where the complexity factor and C_C is given by:

$$C_C = 5.5 \times 10^{-3} (\delta_C + \delta_R) + 7.1 \times 10^{-3} \delta_{pmax}^{1.1}$$

The symbols have the following meaning:

δ_R	= DR	resistor density
N_C	= NC	total number of chips
N_{WB}	= NWB	total number of bonds
D_C	= DC	active and passive chip density
p_{max}	= DX	maximum number of pads found on an IC
$\eta - \eta'$	= N	number of reworks

$\overline{N}_{TRJ} = NTRJ$ average number of transistor junctions per IC

$g_1 = g_1' = G1$ fraction of chips reworked

$g_2 = g_2' = G2$ fraction of bonds reworked

V lot size, one year production

and they are the input variables for the computer programs.

APPENDIX B PROGRAM TO GENERATE A COST SURFACE AND A SINGLE-VALUED COMPLEXITY FACTOR

```

TYPE MATIMO.FOR
00100      DIMENSION IPPN(3), FNAME(5)
00200      DIMENSION COST(50,50)
00300      REAL*8 FILNAM
00400      REAL NWB, N
00500      DATA IFLU/20/
00600      99      FORMAT (' VALUE OF DR ? ', $)
00700      98      FORMAT (' VALUE OF NWB ? ', $)
00800      97      FORMAT (' VALUE OF DC ? ', $)
00900      96      FORMAT (' VALUE OF DX ? ', $)
01000      95      FORMAT (' VALUE OF N ? ', $)
01100      94      FORMAT (' VALUE OF G1 ? ', $)
01200      93      FORMAT (' VALUE OF G2 ? ', $)
01300      92      FORMAT (' VALUE OF V ? ', $)
01400      90      FORMAT('!TEST')
01500      91      FORMAT (' CC= ',F5.3)
01600      89      FORMAT (' ENTER OUTPUT FILE NAME : ', $)
01700      88      FORMAT (5A5)
01800      87      FORMAT('**')
01900      80      FORMAT (50G)
02000
02100      TYPE 89
02200      ACCEPT 88, FNAME
02300      CALL DCDFIL (FNAME, 'ROB', FILNAM, IPPN)
02400      OPEN (UNIT=IFLU, ACCESS='SEQOUT', MODE='ASCII',
02500      IFILE=FILNAM, DIRECTORY=IPPN, DISPOSE='SAVE')
02600      TYPE 99
02700      ACCEPT 80, DR
02800      TYPE 98
02900      ACCEPT 80, NWB
03000      TYPE 97
03100      ACCEPT 80, DC
03200      TYPE 96
03300      ACCEPT 80, DX
03400      TYPE 95
03500      ACCEPT 80, N
03600      TYPE 94
03700      ACCEPT 80, G1
03800      TYPE 93
03900      ACCEPT 80, G2
04000      TYPE 92
04100      ACCEPT 80, V
04200      CC=.0055*(DC+DR)+.0071*DX**1.1
04300      TYPE 91, CC
04400      WRITE(IFLU,90)
04500      DO 75 I=1,50
04600      DO 75 J=1,50
04700      NC=5*I
04800      NTRJ=J*2
04900      75      COST(J,I)=(2.3+.00554*DR+.0093*NC+.004*NWB+.34*CC+NTRJ
05000      1**1*CC*(N*.95+1.38)+N*.025*(G1+G2))*12.*CC*2.5*V**
05100      1(-.4)
05200      WRITE(IFLU,80)COST
05300      WRITE(IFLU,87)
      END

```

APPENDIX C

PROGRAM TO GENERATE A SINGLE-VALUED COST FUNCTION AND COMPLEXITY FACTOR

```

TYPE CSTMOD.FOR
00100      REAL NWB, N
00200      101      FORMAT (' VALUE OF NC ? ', $)
00300      100      FORMAT (' VALUE OF NTRJ ? ', $)
00400      99       FORMAT (' VALUE OF DR ? ', $)
00500      98       FORMAT (' VALUE OF NWB ? ', $)
00600      97       FORMAT (' VALUE OF DC ? ', $)
00700      96       FORMAT (' VALUE OF DX ? ', $)
00800      95       FORMAT (' VALUE OF N ? ', $)
00900      94       FORMAT (' VALUE OF G1 ? ', $)
01000      93       FORMAT (' VALUE OF G2 ? ', $)
01100      92       FORMAT (' VALUE OF V ? ', $)
01200      91       FORMAT (' CC= ', F5.3)
01300      90       FORMAT (' COST = ', F6.2)
01400      80       FORMAT (50G)
01500      TYPE 101
01600      ACCEPT 80, NC
01700      TYPE 100
01800      ACCEPT 80, NTRJ
01900      TYPE 99
02000      ACCEPT 80, DR
02100      TYPE 98
02200      ACCEPT 80, NWB
02300      TYPE 97
02400      ACCEPT 80, DC
02500      TYPE 96
02600      ACCEPT 80, DX
02700      TYPE 95
02800      ACCEPT 80, N
02900      TYPE 94
03000      ACCEPT 80, G1
03100      TYPE 93
03200      ACCEPT 80, G2
03300      TYPE 92
03400      ACCEPT 80, V
03500      CC=.0055*(DC+DR)+.0071*DX**1.1
03600      TYPE 91, CC
03700      COST=(2.3+.00554*DR+.0093*NC+.004*NWB+.34*CC+NTRJ
03800      1**1.1*CC*(N*.95+1.38)+N*.025*(G1+G2))*12.*CC*2.5*V**
03900      1(-.4)
04000      TYPE 90,COST
04100      END

```

APP-D

A-3. Program to generate a single valued cost function and complexity factor by means of a portable programmable calculator.

Input

DR ST01
NC ST02
NWB ST03
DC ST04
DX ST05
NTRJ ST06
N ST07
G1 ST08
G2 ST09
V ST0 0

Coefficients

5.5 10^{-3} ST0.2
9.3 10^{-3} ST0.3
4 10^{-3} ST0.4
CC ST0.5

Program

01 *LEL1	05 14 01	75 RCL0	55 10	70 FRTY	55
02 RCL1	55 01	76 /	51	71 SFO	25 05
03 RCL2	55 10	77 RCL5	55 05	72 RTH	25 17
04 X	51	78 .	57	73 RCL0	54
05 2	02	79 1	01	74 *LEL2	05 14 02
06 .	57	80 *X	15 54	75 RCL4	55 04
07 3	02	81 .	51	76 RCL1	55 01
08 +	41	82 -	41	77 .	41
09 RCL2	55 02	83 RCL5	55 02	78 RCL5	55 15
10 RCL3	55 17	84 RCL5	55 05	79 .	51
11 X	51	85 +	41	80 RCL5	25 05
12 +	41	86 .	57	81 1	01
13 RCL3	55 02	87 0	02	82 .	57
14 RCL4	55 14	88 1	01	83 1	01
15 .	51	89 5	05	84 *X	15 54
16 +	41	90 .	51	85 .	57
17 ST.1	45 11	91 RCL7	55 07	86 0	02
18 SCEL	13 02	92 X	51	87 0	02
19 RCL0	55 10	93 +	41	88 7	07
20 1	01	94 PSE	15 54	89 X	51
21 .	57	95 1	01	90 +	41
22 5	05	96 2	02	91 ST.3	45 10
23 1	51	97 .	57	92 RCL0	55 10
24 RCL1	55 11	98 3	03	93 FRTX	55
25 -	41	99 X	51	94 RTH	25 17
26 RCL7	55 07	00 RCL2	55 10	95 0 0	54
27 .	57	01 .	51		
28 9	09	02 RCL0	55 02		
29 5	05	03 .	57		
30 X	51	04 4	04		
31 1	01	05 CHS	22		
32 .	57	06 1 X	15 54		
33 1	01	07 X	51		
34 +	41	08 2	02		
		09 .	57		
		10 5	05		
		11 .	51		

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR